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Date 12/18/02 Serial # 10/005,697 Priority Application Date 12/14/00

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12-18-02 P02:08 IN

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Other: _____

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Claims 1-11 There are six independent claims

Problem: See Page 2 lines 1-20
" " 3 " 1-12

Solution: " " 3 " 15-20
" " 4 " 1-20

Staff Use Only	Type of Search	Vendors
Searcher: Derrick Blalock	Structure (#)___	STN ✓
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Searcher Location: STIC-EIC2800, CP4-9C18	Litigation___	Questel/Orbit___
Date Searcher Picked Up: 12/20/02 ✓	Fulltext___	Lexis-Nexis___
Date Completed: 12/20/02	Patent Family___	WWW/Internet___
Searcher Prep/Rev Time: 170	Other___	Other ___
Online Time: 60		

FILE 'WPIX, JAPIO'
L1 1 S JP2000-380572/AP,PRN
L2 185 S (MOCHIZUKI, KATSUHISA OR MOCHIZUKI KATSUHISA OR MOCHIZUKI, K OR MOCHIZUKI K)/AU
L3 883604 S DIE OR CHIP OR IC OR ICS OR MICRO(W) CHIP OR MICROCHIP? OR MICROCIRCUIT? OR MICRO(W) CIRCUIT? OR DICE OR WAFER? OR INTEGRATED(W) CIRCUIT? OR LOGIC(W) CIRCUIT?
L4 55068 S (U11-E01/MC OR H01L-021/60/IC)
L5 115224 S ELECTRICAL?(2N) CONDUCT?
L6 158081 S ELECTRICAL?(2N)(CONNECT? OR JOIN? OR LINK? OR CONJOIN?)
L7 78968 S WIR###(2N)(FILM? OR LAYER? OR COAT? OR FLEXIBLE OR ELASTIC OR FLEXILE OR SPRINGY OR FLEXUOUS)
L8 374549 S CIRCLE? OR OVAL OR SPHERE OR CIRCULAR
L9 56504 S SOLID(W) STATE
L10 1009142 S IMAGE OR (S06-A03G1/MC OR H01L-027-14/IC)

L11 380264 S LEAD OR (U11-D03A1A/MC OR H01L-023/495/IC)

L12 1062486 S L10 OR L4
L13 19 S L2 AND L3
L14 4702 S L7 AND L12
L15 184 S L14 AND L5
L16 3 S L15 AND L8
L17 41 S L15 AND HOLE
L18 3 S L16 NOT L13
L19 41 S L17 NOT (L13 OR L16)
L20 883565 S L3 NOT (L13 OR L16 OR L17)
L21 14390 S L20 AND L7
L22 1391 S L21 AND L11
L23 234 S L22 AND L6
L24 2 S L23 AND REFLECT?
L25 3 S L23 AND L10
L26 0 S L23 AND L9
L27 21 S L23 AND L5
L28 2 S L23 AND L8
L29 5 S L23 AND (OPEN OR WINDOW)
L30 26 S L23 AND (OPEN? OR WINDOW)
L31 57 S L21 AND L9
L32 11 S L31 AND L11
L33 39 S L31 AND L10
L34 26 S L24 OR L25 OR L27
L35 11 S L32 NOT (L24 OR L25 OR L27 OR L30)
L36 31 S L33 NOT (L24 OR L25 OR L27 OR L30 OR L32)

L13 ANSWER 1 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2002-557207 [59] WPIX
DNN N2002-441113
TI Flexible wiring film for solid-state image pick-up device e.g. video camera, has hole formed in lead portion which is wider than lead tip and exposed from insulating film.
DC U11 U12
IN **MOCHIZUKI, K**
PA (CANO) CANON KK; (MOCH-I) MOCHIZUKI K
CYC 2
PI US 2002074628 A1 20020620 (200259)* 12p
JP 2002246412 A 20020830 (200273) 8p
ADT US 2002074628 A1 US 2001-5697 20011207; JP 2002246412 A JP 2001-371553 20011205
PRAI JP 2000-380572 20001214
AB US2002074628 A UPAB: 20020916
NOVELTY - The film includes a lead (3) and an insulating film (8). The lead has a hole of shape selected from circle, elongated circle, oval and elongated oval formed in a portion wider than lead tip and exposed from the insulating film. The lead portion contacts with the sealant sealing the lead and an image pick-up element **chip** (2).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Semiconductor apparatus; and
(2) Image pick-up system.
USE - For solid-state image pick-up device such as video camera, digital still camera.
ADVANTAGE - Film adhesion reliability is improved as flexible wiring film is prevented from producing bubbles on leads, as the difference between the flow rates of the sealant is reduced by the formation of hole in the wider lead portion.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic perspective view of solid-state image pick-up device.
Image pick-up element **chip** 2
Lead 3
Insulating film 8
Dwg.1/10

L13 ANSWER 2 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2001-441348 [47] WPIX
DNC C2001-133258
TI Production of multifilament polyester yarn for woven fabrics, free from excessively tight winding, reduced in dispersion of properties in fiber longitudinal direction and in feeling of squeeze.
DC A23 F02
IN MAEDA, Y; **MOCHIZUKI, K**; SUGANO, K
PA (TORA) TORAY IND INC
CYC 25
PI WO 2001036724 A1 20010525 (200147)* JA 26p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: CA CN KR US
JP 2001207329 A 20010803 (200150) 9p
EP 1154055 A1 20011114 (200175) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
KR 2001081027 A 20010825 (200215)
CN 1327492 A 20011219 (200226)
ADT WO 2001036724 A1 WO 2000-JP8040 20001115; JP 2001207329 A JP 2000-330310 20001030; EP 1154055 A1 EP 2000-976251 20001115, WO 2000-JP8040 20001115; KR 2001081027 A KR 2001-706313 20010518; CN 1327492 A CN 2000-802255

20001115
FDT EP 1154055 A1 Based on WO 200136724
PRAI JP 1999-327943 19991118
AB WO 200136724 A UPAB: 20010822
NOVELTY - A multifilament polyester yarn, comprises essentially polytrimethylene terephthalate which has:
(1) a strength in a stress-strain curve of not less than 3 cN/dtex;
(2) a Young's modulus of not more than 25 cN/dtex,;
(3) a minimum differential Young's modulus in the range of 3-10% elongation of not more than 10 cN/dtex; and
(4) an elastic recovery after 10% elongation of not less than 90%.
DETAILED DESCRIPTION - The yarn is free from excessively tight winding even when the spinning yarn is with high speed, has reduced in dispersion of properties in fiber longitudinal direction and in feeling of squeeze to give soft texture.
An INDEPENDENT CLAIM is also included for a process for producing the polyester yarn comprising:
(1) subjecting a polytrimethylene terephthalate with a limiting viscosity (eta) of not less than 0.7 to melt-spinning to form a multifilament yarn;
(2) taking the multifilament yarn up at a spinning rate of not less than 2000 m/min.;
(3) heat-stretching the yarn without temporarily winding up;
(4) successively subjecting the resultant yarn to relaxation treatment at a relaxation degree of 6-12%; and
(5) winding the yarn up to a package.
USE - The method is for the production of multifilament polyester yarn for woven fabrics (claimed).
ADVANTAGE - Such produced yarn is free from excessively tight winding even when spinning yar with high speed, reduced in dispersion of properties in fiber longitudinal direction and in feeling.
DESCRIPTION OF DRAWING(S) - Diagram showing production of polyester yarn with a spinning and stretching device.
Spinning **die** 1
chimney 2
oiling guide 3
first hot roll 4
second hot roll 5
cooling roll 6
interlacing nozzle 7
winding device 8
Dwg.1/4

L13 ANSWER 3 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2001-141998 [15] WPIX
DNN N2001-103782 DNC C2001-042474
TI Semiconductor **integrated circuit** device has insulation film consisting of silicon hydride, having predetermined atom percent of hydrogen formed on electrically conductive film.
DC L03 U11
IN FUKUYAMA, S; INOUE, T; KINOSHITA, T; **MOCHIZUKI, K**; SHIOHARA, M
PA (ADMI) ADVANCED MICRO DEVICES INC; (FUJI-N) FUJITSU AM SEMICONDUCTOR KK; (FUIT) FUJITSU LTD; (FUKU-I) FUKUYAMA S; (INOU-I) INOUE T; (KINO-I) KINOSHITA T; (MOCH-I) MOCHIZUKI K; (SHIO-I) SHIOHARA M
CYC 2
PI JP 2000332008 A 20001130 (200115)* 14p
US 2002038910 A1 20020404 (200227)
ADT JP 2000332008 A JP 1999-140346 19990520; US 2002038910 A1 US 1999-473988 19991229
PRAI JP 1999-140346 19990520
AB JP2000332008 A UPAB: 20010317

NOVELTY - Insulation film consisting of silicon hydride is formed on an electrically conductive film. Hydrogen content in the insulation film is set more than 15.4 atom%. Connection hole is formed on the insulation film for exposing a portion of electrically conductive film. Wiring layer is electrically connected to the electrically conductive film through the connection hole.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the semiconductor **integrated circuit** device manufacturing method.

USE - For semiconductor **integrated circuit** device.

ADVANTAGE - Provides a highly reliable semiconductor device having very less wiring delay. Contributes to the high integration of semiconductor devices easily and reliably.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of multilayer.

Dwg.3/11

L13 ANSWER 4 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2001-016136 [02] WPIX
DNC C2001-004483
TI Computer-aided food extruder cooking control system to regulate dough, water and raw material supplied, applicable in producing direct puff snacks from corn, rice and beans with stable quality and productivity in large quantity.
DC D14
IN **MOCHIZUKI, K**; OGO, K; YAMANE, T
PA (NIRE-N) JAPANESE RES & DEV ASSOC APPLICATION ELE
CYC 91
PI WO 2000069288 A1 20001123 (200102)* JA 32p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000046138 A 20001205 (200113)
EP 1180334 A1 20020220 (200221) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
ADT WO 2000069288 A1 WO 2000-JP3131 20000516; AU 2000046138 A AU 2000-46138 20000516; EP 1180334 A1 EP 2000-927779 20000516, WO 2000-JP3131 20000516
FDT AU 2000046138 A Based on WO 200069288; EP 1180334 A1 Based on WO 200069288
PRAI JP 1999-135695 19990517
AB WO 200069288 A UPAB: 20010110
NOVELTY - A food extruder cooking control method in which a control computer calculates amounts of dough, water and other raw materials for extrusion. Such system has productivity in large quantity, which is operable by one person to control several machines.

DETAILED DESCRIPTION - A food extruder cooking control method in which a control computer calculates specific power consumption for each extruder per unit time which is used as a reference value and the power consumption and the amount of dough supplied, and compares specific power consumption reference value with the actual value, and if the difference is small the revolutions per minute (rpm) of the extruder is controlled, but if such difference is large the rpm as well as the rate of water addition and raw material feeding rate are also controlled so as to ensure a stable quality. An INDEPENDENT CLAIM is also included for a food extruder cooking control system comprising a raw material feeding means, a processing means composed of an extruder, and a control computer.

USE - The system is applicable in producing direct puff snacks from

corn, rice or/and beans.

ADVANTAGE - Such system is computer-aided to regulate dough, water and raw material supplied so that the products have stable quality and productivity in large quantity, which is operable by one person to control several machines.

DESCRIPTION OF DRAWING(S) - Structure of the food extruder cooking control system.

Food extruder cooking control system 1
raw material feeding means 2
water-adding means 3
processing means 4
control computer 5
material tank 20
feeder 21
tank 30
pump 31
pump control 32
hopper 40
heater 41
die 42
motor 43
rotating body 44
product 45
Dwg.1/3

L13 ANSWER 5 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 2000-339319 [29] WPIX
DNC C2000-102900
TI Coating composition useful for producing lubricated metal sheets as materials in car production, with alkaline film-removing properties, chemical conversion treatment properties, blocking resistance and press-moldability.
DC A82 G02 M13
IN GOTOU, Y; HIGAI, K; **MOCHIZUKI, K**; MUKAIHARA, F; OGATA, H; SASAOKA, H; SUZUKI, S; UMINO, S; WAKASA, K
PA (KAWI) KAWASAKI STEEL CORP
CYC 23
PI WO 2000022058 A1 20000420 (200029)* JA 59p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN KR US
JP 2000119558 A 20000425 (200031) 13p
EP 1038933 A1 20000927 (200048) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 2000280400 A 20001010 (200056) 18p
CN 1290287 A 20010404 (200140)
KR 2001033098 A 20010425 (200164)
ADT WO 2000022058 A1 WO 1999-JP5606 19991012; JP 2000119558 A JP 1998-291845 19981014; EP 1038933 A1 EP 1999-970411 19991012, WO 1999-JP5606 19991012; JP 2000280400 A JP 1999-93801 19990331; CN 1290287 A CN 1999-802934 19991012; KR 2001033098 A KR 2000-706461 20000613
FDT EP 1038933 A1 Based on WO 200022058
PRAI JP 1999-93801 19990331; JP 1998-291845 19981014
AB WO 200022058 A UPAB: 20000617
NOVELTY - A coating composition contains a methacrylic resin prepared by copolymerizing (A) strength or a substituted styrene with (B) methacrylic acid ester of a not less than 2C alcohol, and (C) an olefin compound having at least 1 carboxyl group, at a molar ratio of 1:(0.05-44.5):0.12-13).

USE - The coating composition is used to produce metal sheets lubricated by its application (claimed), applicable e.g. in car production.

ADVANTAGE - The thus obtained metal sheets have superior alkaline film-removing properties, chemical conversion treatment properties, coating dryability, blocking resistance, rust-prevention properties, coating stability and press-working properties including powdering resistance and **die** galling resistance.
Dwg.0/0

L13 ANSWER 6 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1999-518011 [43] WPIX
CR 1996-443437 [44]
DNN N1999-385204
TI Heterojunction bipolar transistor (HBT) for light emitting device, light receiving device, **integrated circuits**, etc..
DC U12
IN HIRATA, K; MASUDA, H; **MOCHIZUKI, K**; TANOUE, T; UCHIYAMA, H
PA (HITA) HITACHI LTD; (HISC) HITACHI VLSI ENG CORP
CYC 1
PI US 5949097 A 19990907 (199943)* 30p
ADT US 5949097 A CIP of WO 1995-JP485 19950317, US 1997-932939 19970917
PRAI US 1997-932939 19970917; WO 1995-JP485 19950317
AB US 5949097 A UPAB: 19991020
NOVELTY - A polycrystalline or amorphous undoped GaAs layer (15) is formed on a dielectric Si alloy or Si compound layers (9,14). A through-hole is formed penetrating a dielectric Si layer (17-19) on the GaAs layer, exposing a portion of a conductor layer and the dielectric Si layer. A wiring layer (20) is formed in the through-hole, contacting the conductor layer.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) a communication system;
(b) an electric circuit system; and
(c) a semiconductor device manufacturing method.
USE - E.g. high electric mobility field effect transistors (HEMT), metal Schottky field effect transistor (MESFET), MISFET. Also for memory cell circuits, optical transmission systems, **integrated circuits**, light emitting devices and light receiving devices.
ADVANTAGE - Prevents an electric short-circuit between the conductor layer and a single crystal semiconductor layer, by forming an undoped GaAs semiconductor layer on a dielectric Si alloy or Si compound layer. Reduces the area of a base mesa portion without increasing a base electrode resistance of a semiconductor device. Decreases the wiring capacity by introducing a second dielectric Si alloy layer.
DESCRIPTION OF DRAWING(S) - The figure shows the HBT.
Si alloy or Si compound layer 9,14
Undoped GaAs layer 15
Dielectric Si layer 17-19
Wiring layer 20
Dwg.1/14

L13 ANSWER 7 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1999-401513 [34] WPIX
DNN N1999-300571
TI Electrical operating unit structure for indoor unit of split air conditioner - fixes operation switch panel in operating unit opening of front grill facing front surface of various switches provided in indoor power supply board.
DC Q74 X27
IN **MOCHIZUKI, K**
PA (MATU) MATSUSHITA ELECTRIC IND CO LTD; (MATU) MATSUSHITA DENKI SANGYO KK
CYC 4
PI JP 11159801 A 19990615 (199934)* 6p

CN 1218892 A 19990609 (199941)
US 6189328 B1 20010220 (200112)
ES 2170597 A1 20020801 (200263)
ADT JP 11159801 A JP 1997-327764 19971128; CN 1218892 A CN 1998-123020 19981127; US 6189328 B1 US 1998-198717 19981124; ES 2170597 A1 ES 1998-2501 19981127
PRAI JP 1997-327764 19971128
AB JP 11159801 A UPAB: 19990825
NOVELTY - An operation switch panel (24) which faces the front surface of various switches (23) arranged in an indoor power supply board (22) is guided and inserted in the opening (26) of an operating unit (25) formed in a front grill (5) which comprises the suction inlet and outlet of internal room air in the main body (1) of an indoor unit. DETAILED DESCRIPTION - An indoor heat exchanger and an indoor air blower are accommodated inside the main body of the indoor unit to generate an indoor style of air conditioning. An outdoor unit provided with an outdoor heat exchanger and an outdoor air blower which generate an outdoor style between an outdoor suction inlet and an outdoor outlet in an outdoor unit main body with an outdoor power supply board is connected through a refrigerating cycle and an electric wiring circuit to the indoor unit.
USE - For accommodating operation switch panel in the operating unit of an indoor unit.
ADVANTAGE - The operativity improves since various switches of a power supply board can be operated easily from the operating unit opening of the front grill. The quality of the products can be stabilized and arranged easily in the position of design size. An abnormal stress or biting to the various switches during the attachment can be prevented since the operation switch panel is located face to face with the power supply board. The shape of a **die** for molding the front grill can be simplified and the **die** size can be made small since the need to form complicated holes for various switches and sliding mechanism of an operating unit in the front grill is eliminated by providing an operation switch panel. DESCRIPTION OF DRAWING(S) - The drawing is an exploded perspective view showing the indoor unit main body of a split type air conditioner. (1) Main body; (5) Front grill; (22) Indoor power supply board; (23) Various switch; (24) Operation switch panel; (25) Operation unit; (26) Opening.
Dwg.1/7

L13 ANSWER 8 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1998-419809 [36] WPIX
DNN N1998-327539
TI Semiconductor device e.g. **IC**, LSIC - includes first insulating film to which second insulating film is adhered in such way that density of substance of second insulating film is different at adhesion surface than other surfaces.
DC U11
IN BURKI, I; CHAN, S; HUANG, R; IMAOKA, K; **MOCHIZUKI, K**; NUKUI, K; TANIGUCHI, T
PA (ADMI) ADVANCED MICRO DEVICES INC; (FUJI-N) FUJITSU AMD SEMICONDUCTOR KK; (FUIT) FUJITSU LTD; (FUJI-N) FUJITSU AM SEMICONDUCTOR KK
CYC 4
PI JP 10173052 A 19980626 (199836)* 14p
TW 356587 A 19990421 (199936)
KR 98063322 A 19981007 (199949)
US 6232663 B1 20010515 (200129)
KR 323622 B 20020308 (200262)
ADT JP 10173052 A JP 1996-334141 19961213; TW 356587 A TW 1997-108764 19970623; KR 98063322 A KR 1997-21482 19970529; US 6232663 B1 US 1997-904630 19970801; KR 323622 B KR 1997-21482 19970529
FDT KR 323622 B Previous Publ. KR 98063322

PRAI JP 1996-334141 19961213
AB JP 10173052 A UPAB: 19980911
The device includes a first insulating film (2) which is formed on the surface of a substrate. A second insulating film (3) which contains a substance whose density at adhesion surface is different from that of other surface, is adhered to first insulating film.
ADVANTAGE - Improves reliability of insulating film. Improves formation technique of contact hole for electro formation. Improves yield. Prevents micro defects in insulating film.
Dwg.1/17

L13 ANSWER 9 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1996-052350 [06] WPIX
TI Measuring probe for both LF and HF measurements esp. on **IC** and VLSI circuits - has LF and HF device alternately connected to line, third conductor running parallel to line, and resistance and capacitance between probe end and common conductor using switch to change between HF and LF measurements.
DC S01 U11
IN HABU, S; **MOCHIZUKI, K**
PA (YOKH) YOKOGAWA HEWLETT PACKARD LTD; (HEWP) HEWLETT-PACKARD CO
CYC 2
PI JP 07218544 A 19950818 (199606)* 7p
US 5680039 A 19971021 (199748)B 12p
US 5903143 A 19990511 (199926)
ADT JP 07218544 A JP 1994-32875 19940204; US 5680039 A US 1995-382501 19950202; US 5903143 A Div ex US 1995-382501 19950202, US 1997-868381 19970603
FDT US 5903143 A Div ex US 5680039
PRAI JP 1994-32875 19940204
AB US 5680039 A UPAB: 19971209 ABEQ treated as Basic
The probe for device under test (DUT) (50) comprises a line having two conductors and two ends. A common conductor is connected to ground. A series connected resistor-capacitor circuit is connected between the common conductor and the second conductor at the second end of the line. The switch is connected to the first conductor and second conductor at the first end of the line and configured in one state when the probe apparatus is employed for HF signal measurements. The first state connects the first conductor of the line to a signal-carrying conductor of HF line and connects the second conductor to a ground connection.
The switch is configured in a second state when the probe is employed for LF measurements. The second state connects the first conductor to a signal-carrying conductor of an LF line and connects the second conductor to a guard conductor forming a portion of the LF line. Components include pulse sources (102,104), output resistor (103), resistor (105) and load (106).
USE/ADVANTAGE - For both high and low frequency signal measurements. Inexpensive probe.
Dwg.4B/6
AB JP 07218544 A UPAB: 19990525
The probe for device under test (DUT) (50) comprises a line having two conductors and two ends. A common conductor is connected to ground. A series connected resistor-capacitor circuit is connected between the common conductor and the second conductor at the second end of the line. The switch is connected to the first conductor and second conductor at the first end of the line and configured in one state when the probe apparatus is employed for HF signal measurements. The first state connects the first conductor of the line to a signal-carrying conductor of HF line and connects the second conductor to a ground connection.
The switch is configured in a second state when the probe is employed for LF measurements. The second state connects the first conductor to a

signal-carrying conductor of an LF line and connects the second conductor to a guard conductor forming a portion of the LF line. Components include pulse sources (102,104), output resistor (103), resistor (105) and load (106).

USE/ADVANTAGE - For both high and low frequency signal measurements. Inexpensive probe.

L13 ANSWER 10 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1995-217653 [29] WPIX
DNC C1995-100580
TI Potato crisps or **chips** prodn. - by cutting, frying, freezing, frying and drying so that they can be marketed with no refrigeration.
DC D13
IN MAKISHIMA, S; **MOCHIZUKI, K**
PA (MEIJ) MEIJI SEIKA KAISHA LTD
CYC 3
PI GB 2284973 A 19950628 (199529)* 25p
JP 07184587 A 19950725 (199538) 9p
GB 2284973 B 19970820 (199736)
US 5700508 A 19971223 (199806) 10p
JP 2931517 B2 19990809 (199937) 9p
ADT GB 2284973 A GB 1994-26195 19941223; JP 07184587 A JP 1993-331552 19931227; GB 2284973 B GB 1994-26195 19941223; US 5700508 A US 1994-363877 19941227; JP 2931517 B2 JP 1993-331552 19931227
FDT JP 2931517 B2 Previous Publ. JP 07184587
PRAI JP 1993-331552 19931227
AB GB 2284973 A UPAB: 19950727
Fried potatoes are mfd. by (a) cutting potatoes into pieces; (b) blending in 60-70 deg.C water for 5-10 minutes; (c) primary frying in edible oil at 160-190 deg. C; (d) immediately freezing at -20 deg. C or below; (e) secondary frying of the frozen pieces in edible oil at 170-190 deg. C; and (f) drying. Prods. contain 0.5-5 w t.% moisture and 30-35 wt.% fat.

ADVANTAGE - Prods. have a stick or corrugated form, a crispy and softy taste (sic.) and can be marketed with no refrigeration.
Dwg.4/4

L13 ANSWER 11 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1994-344975 [43] WPIX
CR 1994-327625 [41]
DNN N1994-270766 DNC C1994-156978
TI Forming semiconductor thin film on semiconductor **wafer** in prodn. of transistor - by covering **wafer** with patterned mask, forming aluminium or indium arsenide layer and depositing GP-III-V semiconductor film.
DC L03 U11
IN FUJISAKI, Y; HAGA, T; MASUDA, H; MISHIMA, T; **MOCHIZUKI, K**; NAKAMURA, T; TANOUE, T
PA (HITA) HITACHI LTD
CYC 2
PI JP 06267865 A 19940922 (199443)* 12p
US 5481120 A 19960102 (199607) 62p
ADT JP 06267865 A JP 1993-53722 19930315; US 5481120 A US 1993-164801 19931210
FDT US 5481120 A JP 06252163
PRAI JP 1993-53722 19930315; JP 1992-347688 19921228
AB JP 06267865 A UPAB: 19970909
Process includes covering a **wafer** with a patterned mask, forming Al arsenide or In arsenide layer on the **wafer** by organo-metal CVD, and depositing a Gp III-V cpd.-semiconductor thin film contg. C.

USE/ADVANTAGE - A thin film of less than 100 microns in thickness may be formed easily.
Dwg.1/9

L13 ANSWER 12 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1994-327625 [41] WPIX
CR 1994-344975 [43]
DNN N1994-257482 DNC C1994-148836
TI Forming semiconductor thin film on semiconductor **wafer** in prodn. of transistor - by covering **wafer** with patterned mask, forming aluminium or indium arsenide layer and depositing GP-III-V semiconductor film.
DC L03 U11
IN FUJISAKI, Y; HAGA, T; MASUDA, H; MISHIMA, T; **MOCHIZUKI, K**; NAKAMURA, T; TANOUE, T
PA (HITA) HITACHI LTD
CYC 2
PI JP 06252163 A 19940909 (199441)* 34p
US 5481120 A 19960102 (199607) 62p
ADT JP 06252163 A JP 1993-276484 19931105; US 5481120 A US 1993-164601 19931210
FDT US 5481120 A JP 06252163
PRAI JP 1992-347688 19921228; JP 1993-53722 19930315
AB JP 06252163 A UPAB: 19970909
Dwg.1/69

L13 ANSWER 13 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1990-350087 [47] WPIX
DNN N1990-267427 DNC C1990-151937
TI Flexible plastic data carrier apparatus - used in controlling unmanned spinning mills.
DC A85 F02 T01 T04 U11 W02 X25
IN MASUDA, H; **MOCHIZUKI, K**; YAGI, T
PA (STAR-N) STAR MICRONICS CO L
CYC 5
PI EP 398301 A 19901122 (199047)*
R: CH DE IT LI
JP 02305233 A 19901218 (199105)
EP 398301 A3 19921202 (199343)
ADT EP 398301 A EP 1990-109262 19900516; JP 02305233 A JP 1989-126463 19890519; EP 398301 A3 EP 1990-109262 19900516
PRAI JP 1989-126463 19890519
AB EP 398301 A UPAB: 19931207
A moveable data carrier appts. (I) for transmitting and receiving data from a non-contacting fixed scanner is claimed comprising a reception coil coaxially fitted into a moving holder (II), a transmitting antenna attached (pref. coaxially) to (II) and an **IC** in close contact with (II). Pref. (II) is a hollow cylinder (partic. a yarn spool) and the data carrier is composed of a flexible substrate (III) (pref. a polyamide or polyester film) bearing the data receivers and transmitters, (III) being folded and inserted inside (II).

A method for mfg. (I) is also claimed comprising attaching (III) with its associated transmitters/receivers to the outer surface of a hollow cylinder, inserting this cylinder into an outer cylinder, pouring a molten resin into the inner cylinder, placing the assembly in a vacuum chamber, removing air from the inner cylinder so allowing the resin to flow into the space between the two cylinders through a hole on the side of the inner cylinder, allowing the resin to solidify and then shaping the prod. so obtd..

USE/ADVANTAGE - (I) can be used in the automatic control of a spinning mill. The functional stability of the elements of (I) is enhanced. @(19pp Dwg.No.1/12)@
1/12

L13 ANSWER 14 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1989-267173 [37] WPIX
TI Atomic layer epitaxy for **IC** device mfr. - by applying gallium cpd. vapour onto substrate, annealing, and directing arsenic cpd. particle NoAbstract Dwg 1/4.
DC L03 U11
IN **MOCHIZUKI, K**; OHTSUKA, N; OZEKI, M
PA (FUIT) FUJITSU LTD
CYC 2
PI JP 01194318 A 19890804 (198937)* 3p
US 5166092 A 19921124 (199250)B 17p
JP 2705726 B2 19980128 (199809) 8p
ADT JP 01194318 A JP 1988-18393 19880128; US 5166092 A Cont of US 1989-302651 19890127, US 1990-608602 19901030; JP 2705726 B2 JP 1988-18393 19880128
FDT JP 2705726 B2 Previous Publ. JP 01194318
PRAI JP 1988-18393 19880128

L13 ANSWER 15 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1989-208204 [29] WPIX
DNN N1989-158785 DNC C1989-092345
TI Non-resonant vibration sensor with piezoelectric element - has piezoelectric conversion portion and lead wire member integrally covered with polyamide resin.
DC A85 S02 V06 X22
IN **MOCHIZUKI, K**
PA (DENK) TDK CORP
CYC 5
PI EP 324187 A 19890719 (198929)* EN 11p
R: DE FR GB IT
US 4966031 A 19901030 (199046)
EP 324187 B1 19930324 (199312) EN 9p
R: DE FR GB IT
DE 3879662 G 19930429 (199318)
ADT EP 324187 A EP 1988-121914 19881230; US 4966031 A US 1989-294073 19890106; EP 324187 B1 EP 1988-121914 19881230; DE 3879662 G DE 1988-3879662 19881230, EP 1988-121914 19881230
FDT DE 3879662 G Based on EP 324187
PRAI JP 1988-1800U 19880111
AB EP 324187 A UPAB: 19930923
The vibration sensor includes a base member shaped in the form of a sleeve having a structure for installation on an object of measurement, a piezoelectric conversion portion put onto the periphery of the same, and lead wire member connecting the same with the outside of the sensor. The device is characterized in that the piezoelectric conversion portion and a portion of the lead wire member are integrally covered with polyamide resin and it is thereby formed into a case member.

The device makes most of the characteristics of the polyamide resin having a strong crystalline polymer structure.

ADVANTAGE - Frequency response characteristic of vibration sensor is improved against thermal stress.

1/6

L13 ANSWER 16 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1985-271037 [44] WPIX
DNN N1985-202371
TI Fuel injection system for multi-cylinder **IC** engine - has cylinders divided into at least two groups to give graduated fuel switch off.
DC Q52 X22
IN **MOCHIZUKI, K**
PA (FUJH) FUJI JUKOGYO KK

CYC 2
PI DE 3513656 A 19851024 (198544)* 11p
GB 2157853 A 19851030 (198544)
GB 2157853 B 19870909 (198736)
ADT DE 3513656 A DE 1985-3513656 19850416; GB 2157853 A GB 1985-9823 19850417
PRAI JP 1984-78168 19840417
AB DE 3513656 A UPAB: 19930925
The appts. includes a unit for the production of an r.p.m. signal corresp. to the rotational speed of the engine and a second unit which produces a signal corresp. to the closing of the throttle valve. The fuel injection units are divided into at least two groups and a comparator compares the engine r.p.m. signal with a first r.p.m. signal for switching off the fuel supply, and a second r.p.m. signal lower than the first signal for restoring the fuel supply.

A fuel switch-off circuit, responds to the throttle valve signal and the comparator output signals, to produce a fuel switch off signal if the engine r.p.m. signal is lower than the first signal, and to produce a fuel restoring signal if the engine r.p.m. signal is lower than the second r.p.m. signal. A selector responds to the fuel switch off signal, to select and switch off the fuel to one group, whilst the other group has a delayed switch off. The restoring of the fuel supply responds to the fuel supply restoring signal.

ADVANTAGE - Has ignition units operated in stages so that number of working cylinders is gradually reduced.
1/3

L13 ANSWER 17 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1984-116373 [19] WPIX
DNN N1984-086008
TI **IC** engine fuel injection system - decreases injection time delay w.r.t. increase of engine speed, and has maximum time delay selected after intake valves have closed.
DC Q52 Q53 X22
IN **MOCHIZUKI, K**
PA (FUJH) FUJI JUKOGYO KK
CYC 3
PI GB 2129051 A 19840510 (198419)* 8p
DE 3335637 A 19840510 (198420)
US 4512316 A 19850423 (198519)
GB 2129051 B 19860326 (198613)
DE 3335637 C 19880407 (198814)
ADT GB 2129051 A GB 1983-25843 19830927; DE 3335637 A DE 1983-3335637 19830930; US 4512316 A US 1983-538467 19831003
PRAI JP 1982-173630 19821001
AB GB 2129051 A UPAB: 19930925
The system has intake valves, fuel injection valves, and control unit for deciding fuel injection time and fuel injection duration. A fuel injection time delay signal is produced representing a delay after ignition time, that time delay decreasing with increase of the engine speed. A max. time delay is selected to inject fuel after intake valves of the engine have closed so that the fuel injection valve is opened by the fuel injection signal for injecting fuel.

The delay signal is applied to an adder circuit, alternatively the pulses from an oscillator are counted and the output is applied to the adder and a comparator. The output of the adder is stored in a register, this representing the fuel injection time delay. When the counter coincides with the register, the comparator produces a fuel injection signal and a reset signal.
5/5

L13 ANSWER 18 OF 19 WPIX (C) 2002 THOMSON DERWENT

AN 1983-742261 [34] WPIX
DNN N1983-146857
TI **IC** engine fuel injection system - uses trigger signal for fuel injection obtained from ignition signal.
DC Q52 Q53 X22
IN **MOCHIZUKI, K**
PA (FUJH) FUJI HEAVY IND LTD
CYC 6
PI DE 3304473 A 19830818 (198334)* 10p
GB 2114659 A 19830824 (198334)
FR 2521222 A 19830812 (198337)
AU 8311282 A 19830818 (198340)
GB 2114659 B 19850731 (198531)
DE 3304473 C 19860403 (198615)
CA 1202404 A 19860325 (198617)
US 4768488 A 19880906 (198838)
ADT GB 2114659 A GB 1983-3723 19830210; US 4768488 A US 1987-64834 19870619
PRAI JP 1982-20757 19820210
AB DE 3304473 A UPAB: 19930925
The fuel injection system has at least one fuel injection valve opened under control of a fuel injection signal provided by a regulator. The engine ignition pulses are fed to a frequency divider for providing a synchronous trigger signal used for control of the fuel injection signal so that injection is effected when the intake valves of the coupled cylinder are closed. Pref. the regulator uses a microcomputer (6) coupled to a read-only memory (7), a data interface (8) and an A/D converter (12). The data interface (8) is supplied with the ignition signal (IGN) obtained from the distributor, an air flow signal (AFM) from a sensor positioned in the air intake, an exhaust emission level signal provided by an oxygen sensor incorporated in the exhaust pipe and a signal from a temp. monitor incorporated in the engine cooling circuit.
2/5

L13 ANSWER 19 OF 19 WPIX (C) 2002 THOMSON DERWENT
AN 1978-L2554A [51] WPIX
TI Magnetic recording and reproducing appts. using cassette - has magnetic head in contact with tape at reproduce position by use of pinch roller and capstan.
DC T03
IN **MOCHIZUKI, K**
PA (BANI-I) BAN I
CYC 1
PI US 4129889 A 19781212 (197851)*
PRAI JP 1976-61794 19760529; JP 1976-107906 19760910; JP 1976-130471 19761101
AB US 4129889 A UPAB: 19930901
In a magnetic recording/reproducing apparatus having a support which reciprocates between reproduce and stop positions and is biased by a spring in the direction of the reproduce position, a magnetic head is mounted such that **ic** contacts with a magnetic tape at the reproduce position and disengages from the magnetic tape at the stop position.

The head is mounted on the support and a pinch roller is mounted where it can be depressed against a capstan at the reproduce position. The pinch roller is removed from the capstan at the stop position on the support or on a deck. The pinch roller is also biased by a spring in the direction of the capstan.

L18 ANSWER 1 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 2002-317250 [36] WPIX
DNN N2002-248383 DNC C2002-092310
TI Semiconductor package for use in electronic products, e.g. personal computers, includes implantable **conductive** lands **electrically** connected to bond pad of semiconductor chip.
DC A32 A85 L03 U11
IN GANG, H; KANG, H S
PA (KOST-N) KOSTAT SEMICONDUCTOR CO LTD; (GANG-I) GANG H
CYC 29
PI EP 1179844 A2 20020213 (200236)* EN 31p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
CN 1337741 A 20020227 (200236)
JP 2002057241 A 20020222 (200236) 17p
US 2002041019 A1 20020411 (200236)
US 6429508 B1 20020806 (200254)
KR 2002012901 A 20020220 (200257)
ADT EP 1179844 A2 EP 2000-309247 20001020; CN 1337741 A CN 2000-131634 20001020; JP 2002057241 A JP 2000-331153 20001030; US 2002041019 A1 Div ex US 2000-677598 20001003, US 2001-12480 20011212; US 6429508 B1 US 2000-677598 20001003; KR 2002012901 A KR 2000-46164 20000809
PRAI KR 2000-46164 20000809
AB EP 1179844 A UPAB: 20020610
NOVELTY - A semiconductor package comprises (a) a semiconductor package body (101) which is formed of a sealing resin (104) and which includes a semiconductor chip (100) with bond pads but without a lead frame or a substrate; and (b) implantable conductive lands (112, 114) attached to the package body to be exposed to the outside, each being electrically connected to a bond pad of the semiconductor chip.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of manufacturing the above semiconductor package, comprising:

(a) attaching a semiconductor chip to a temporary substrate, in which the implantable conductive lands are formed on a tape film (110),

(b) molding the temporary substrate, and

(c) detaching the tape film from the molded resultant structure.

USE - For use in electronic products, e.g. personal computers, cellular phones or camcorders.

ADVANTAGE - The inventive semiconductor package has improved electrical, thermal and mechanical performance. It can be manufactured by simple methods at reduced cost.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view for explaining the structure of the inventive semiconductor package.

Semiconductor chip 100
Semiconductor package body 101
Die-bonding epoxy 102
Sealing resin 104
Wires 106
Tape film 110
Implantable conductive lands 112, 114
Dwg.10/34

L18 ANSWER 2 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 1997-356936 [33] WPIX
DNN N1997-296270
TI Manufacturing method of ceramic circuit substrate used as component in e.g. computer, mobile communication, game machine, **image** processor - by performing blast treatment to remove thin-line path between **electrically-conductive** polar zone after performing

electroplating to polar zone and **wiring layer**.

DC U11 U14 V04
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 09148716 A 19970606 (199733)* 7p
ADT JP 09148716 A JP 1995-302736 19951121
PRAI JP 1995-302736 19951121
AB JP 09148716 A UPAB: 19970813
The method involves the formation of a circuit layer and **electrically-conductive** polar zones (2) on the top surface of a ceramic substrate (1). A thin-line path (3) is electrically connected between polar zones.

Electroplating is performed to the polar zones and the **wiring layer** using the thin-line path. The thin-line path is removed after an appropriate time by performing blast treatment.

USE/ADVANTAGE - Used in e.g. machine-tool control apparatus, industrial apparatus controller. Enables obtaining superior ceramic circuit substrate with high operational reliability. Reduces generation of mixed signal when high-speed signa and high frequency signal are processed. Needs no use of plating leader when performing electroplating. Prevents danger of short circuit after mounting. Improves electric insulation between polar zones. Prevents generation of crack to substrate since intensity is not reduced even if insulated trough formed through blast treatment has **circular** cross section.
Dwg.2/3

L18 ANSWER 3 OF 3 WPIX (C) 2002 THOMSON DERWENT
AN 1996-274872 [28] WPIX
DNN N1996-231258
TI Ball grid array semiconductor package for LSI - has spherical conductive incandescent lamp attached to conductive material which does not dissolve during mounting.
DC U11
PA (HISC) HITACHI CHO LSI ENG KK; (HITA) HITACHI LTD
CYC 1
PI JP 08115997 A 19960507 (199628)* 8p
ADT JP 08115997 A JP 1994-246634 19941013
PRAI JP 1994-246634 19941013
AB JP 08115997 A UPAB: 19960719
The device includes a semiconductor substrate formed with a conductive region (5). The conductive region is connected to several terminals of a semiconductor chip (1) through a bonding wire (6). The terminals at the chip are attached using an adhesive agent **coated** on a **wiring** board (3).

The **electrically conductive** region is formed with a wiring pattern which is extended from the surface of a wiring board up to the back side. The back side contg. the conductive material is attached to a spherical incandescent lamp covered with an **electrically conductive** layer (9) which does not dissolve during mounting.

ADVANTAGE - Reliable for mounting since bump not connected to **electrically conductive** surface of substrate during mounting. Uniformly maintains dia. of spherical incandescent lamp during mounting. Does not generate poor bridge even with reduced bump height since distance between conductive incandescent lamps is kept uniform. Does not increase mounting cost since inspection number of processes does not increase. Improves reliability of mounting since heat fatigue resistance of connected portion is long.
Dwg.1/10

L19 ANSWER 1 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-522759 [56] WPIX
DNN N2002-413706
TI Manufacturing method for electro-optical device, involves drilling and connecting contact **holes** between **electrically conductive** film of shading **film wiring** and insulating **film** in **image** display area.
DC P81 P85 U11 U14
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 2002108244 A 20020410 (200256)* 25p
ADT JP 2002108244 A JP 2000-294325 20000927
PRAI JP 2000-294325 20000927
AB JP2002108244 A UPAB: 20020903
NOVELTY - The method involves drilling a series of contact **holes** which connect simultaneously between a peripheral circuit or a peripheral wiring, and a shading **film wiring** in a peripheral area. Afterwards, the contact **holes** are connected between the **electrically conductive** film of the shading **film wiring** and an insulating film in an **image** display area.
USE - For electro-optical device e.g. liquid-crystal device.
ADVANTAGE - Ensures efficient manufacture of the electro-optical device even with comparatively complicated structure.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the electro-optical device. (Drawing includes non-English language text)
Dwg.3/24

L19 ANSWER 2 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-292467 [33] WPIX
DNN N2002-228345
TI Two-metal TAB tape, double-sided CSP tape, BGA tape, and method for manufacturing the same.
DC U11
IN HAYASHI, K; ICHIRYU, A; ISHII, M; KATAOKA, T; KAWAMURA, H
PA (MITG) MITSUI MINING & SMELTING CO; (MITG) MITSUI MINING & SMELTING CO LTD
CYC 23
PI WO 2002023617 A1 20020321 (200233)* JA 16p <--
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: KR US
JP 2002093861 A 20020329 (200238) 6p <--
EP 1235267 A1 20020828 (200264) EN <--
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
ADT WO 2002023617 A1 WO 2001-JP7834 20010910; JP 2002093861 A JP 2000-276051 20000912; EP 1235267 A1 EP 2001-963556 20010910, WO 2001-JP7834 20010910
FDT EP 1235267 A1 Based on WO 200223617
PRAI JP 2000-276051 20000912
AB WO 200223617 A UPAB: 20021031
NOVELTY - A two-metal TAB tape, double-sided CSP tape, and BGA tape in which the tape has an insulating substrate and **wiring layers** at least on both sides of the insulating substrate, sprocket **holes** are made at regular intervals in the longitudinal direction along the edges in the direction of width, through **holes** are made in the substrate by punching press, the through **holes** are filled with conductor by punching press, and the **conductor** is **electrically** connected to the **wiring layers** , characterized in that pilot round **holes** are made among the sprocket **holes** made in the longitudinal direction. Methods for producing such two-metal TAB tape, double-sided CSP tape, and BGA tape are disclosed.
USE - Two-metal TAB tape, double-sided CSP tape, BGA tape, and method

for manufacturing the same
Dwg.1/3

L19 ANSWER 3 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2002-008062 [01] WPIX
DNN N2002-007152
TI Film carrier for printed wiring board of TV, radio, has thin film conductor layer formed on both sides of conduction **holes** in insulating film by sputtering.
DC U11
PA (TOPP) TOPPAN PRINTING CO LTD
CYC 1
PI JP 2001291746 A 20011019 (200201)* 5p <--
ADT JP 2001291746 A JP 2000-102596 20000404
PRAI JP 2000-102596 20000404
AB JP2001291746 A UPAB: 20020105
NOVELTY - A thin film conductor layer (4) is formed on both sides of conduction **holes** (7) in insulating **film** by sputtering. **Wiring layers** (6a,6b) connected **electrically** through **conduction holes** (7), are formed on both sides of sprocket **holes** (2) and insulating film (1) along longitudinal direction, contacting the layer (4).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for film carrier manufacturing method.
USE - Used in printed wiring board of industrial electronic devices, consumer electronic devices such as television, mobile telephone, game machine, radio, audio equipment, VTR, electronic computer, OA apparatus, electronic application apparatus, electric measuring device, communication apparatus.
ADVANTAGE - Since a thin film conductor layer is formed on both sides of conduction **holes** by sputtering, electric connection reliability between **wiring layers** of insulating film becomes high. Manufacturing process of the film carrier is simplified.
DESCRIPTION OF DRAWING(S) - The figure shows sectional views explaining the film carrier manufacturing process.
Insulating film 1
Sprocket **holes** 2
Thin film conductor layer 4
Wiring layers 6a,6b
Conduction **holes** 7
Dwg.2/4

L19 ANSWER 4 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-411690 [44] WPIX
DNN N2001-304483 DNC C2001-124708
TI Flat tape for double sided wiring tape automated bonding - has **electrically conductive** layer whose one end is connected to copper laminated signal layer and other to mounting area of solder ball.
DC A85 L03 U11
PA (HITD) HITACHI CABLE LTD
CYC 1
PI JP 11121539 A 19990430 (200144)* 6p <--
ADT JP 11121539 A JP 1997-288326 19971021
PRAI JP 1997-288326 19971021
AB JP 11121539 A UPAB: 20010815
NOVELTY - A copper laminate signal layer (22) with thickness 20 mu m or less is formed below a base film (21). Ends of an **electrically conductive** layer are connected to the signal layer and to mounting area of solder ball (23), respectively. The base film has a **hole** (24) with 100 mu m or less of wiring pitch for connecting **wiring**

layer with both surfaces of the base film. DETAILED DESCRIPTION - A copper laminate wiring pattern of pitch 100 mu m or less is formed on one surface of a base film (21) and to its another surface a power supply layer (23) is formed with same wiring pitch and thickness.

USE - For double sided wiring tape automated bonding (TAB) for QFP, BGA type semiconductor packages.

ADVANTAGE - Since the thickness of **wiring layer** is made below predetermined value, stable, cheap and reliable tape is obtained with superior insulation resistance. A flat tape is enhanced since carbon dioxide laser is used to perform drilling of blind via **hole**. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of flat tape for double sided wiring TAB. (21) Base film; (22) Copper laminate signal layer; (23) Solder ball; (24) **Hole**.
Dwg.1/5

L19 ANSWER 5 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-268601 [28] WPIX
DNN N2001-192322 DNC C2001-081702
TI Copper wiring formation on substrate for wireless modem, involves forming titanium and copper layers on substrate, coating photoresist and photomask on copper layer, exposing and developing exposed pattern.
DC A85 G06 L03 V04
PA (TONG-N) TONGXIN ELECTRONIC IND CO LTD
CYC 1
PI JP 2001044603 A 20010216 (200128)* 4p
ADT JP 2001044603 A JP 1999-201437 19990715
PRAI JP 1999-201437 19990715
AB JP2001044603 A UPAB: 20010522
NOVELTY - Formation of copper (Cu) wiring (CW) on substrate by electrode plating, involves forming titanium and Cu layers on substrate on which through-**hole** is formed, coating photoresist containing crosslinkable resin and positive type photomask on Cu layer, exposing and developing the uncovered wiring pattern (WP) areas, forming Cu wiring on molding frame of WP, peeling the layers and forming plated layers on CW.

DETAILED DESCRIPTION - Titanium and copper layers are sequentially formed on a substrate on which through **hole** is formed, by sputtering method. A photoresist containing resin which performs crosslinking reaction by ultraviolet rays, is coated on the copper **layer** on which **wiring** is to be formed. The positive type photomask is formed on photoresist layer in the area where wiring pattern is formed. The crosslinking reaction of photoresist in the area not covered by wiring pattern is performed by exposure using ultraviolet rays. The molding frame of the wiring pattern is formed on copper layer by **image** developing process which is performed by removing the area where the crosslinking reaction is not performed, using developer liquid. The copper wiring is formed on molding frame of wiring pattern with the copper coating. The photoresist layer which remains on surface of substrate is peeled, and the copper and titanium layers are sequentially removed. The nickel and gold plated layers are sequentially formed on the surface of copper wiring.

USE - For forming copper wiring on the substrate by electroplating for radio equipment such as cellular local area network (LAN), wireless LAN and wireless modem.

ADVANTAGE - The copper wiring formed is thin, straight and is excellent in flatness. The copper wiring has high density. The copper wiring excels in electric **conduction** efficiency, **electrical** property, stability, high frequency characteristics and physical characteristics. Manufacturing cost of the wiring is minimized. The copper wiring has high industrial value.

DESCRIPTION OF DRAWING(S) - The figure shows flow chart of the formation of copper wiring on the substrate by electroplating. (Drawing

includes non-English language text).
Dwg.1/2

L19 ANSWER 6 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2001-126851 [14] WPIX
DNN N2001-093597
TI Solid state **image** pick-up in scanner, has contact **holes** on upper surface of forwarding and shift electrodes so that electrodes contact respective **wiring layers** through conductive material filled inside **holes**.
DC U13 W04
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 2000223689 A 20000811 (200114)* 10p
ADT JP 2000223689 A JP 1999-26482 19990203
PRAI JP 1999-26482 19990203
AB JP2000223689 A UPAB: 20010312
NOVELTY - The contact **holes** (9a,7a) are formed on upper surface of the forwarding electrode (31) of CCD register and shift electrode (2b), respectively. The **wiring layers** (6,8) are connected to respective electrodes through **electrically conductive** material filled inside the **holes**.
USE - Solid state **image** pick-up in scanner.
ADVANTAGE - Eliminates entering of the ambient light into the CCD register, as ambient light is interrupted by contact **holes**, thereby offering solid state **image** pick-up with outstanding electrical property and increased S/N ratio.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of solid state **image** pick-up.
Shift electrode 2b
Wiring layers 6,8
Contact **holes** 7a,9a
Forwarding electrode 31
Dwg.1/13

L19 ANSWER 7 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-677040 [66] WPIX
DNN N2001-237074 DNC C2001-101094
TI Chip scale package structure for electronic device, information apparatus - forms conductive pattern on lower surface of insulating plate so that wire bonding is exposed in **hole**.
DC L03 U11
IN KIM, J H; SEONG, S C; KIM, J; SUNG, S
PA (SMSU) SAMSUNG ELECTRONICS CO LTD; (KIMJ-I) KIM J; (SUNG-I) SUNG S
CYC 3
PI KR 99085107 A 19991206 (200066)*
JP 11354572 A 19991224 (200135)B 10p <--
US 2002003308 A1 20020110 (200208)
KR 292033 B 20010712 (200226)
ADT KR 99085107 A KR 1998-17262 19980513; JP 11354572 A JP 1999-130074 19990511; US 2002003308 A1 US 1999-310466 19990512; KR 292033 B KR 1998-17262 19980513
FDT KR 292033 B Previous Publ. KR 99085107
PRAI KR 1998-17262 19980513
AB JP 11354572 A UPAB: 20010625 ABEQ treated as Basic
NOVELTY - A semiconductor chip and insulating plate with a penetration **hole** (12) are bonded together by adhesive agent (3). A conductive pattern is formed on the lower surface of the insulating plate so that the wire bonding is exposed in the **hole**. A bonding wire (5) connects a bonding pad and the **conductive** pattern, **electrically**
. DETAILED DESCRIPTION - A sealing portion (7) seals the semiconductor

chip in order to protect from external environment. An INDEPENDENT CLAIM is also included for semiconductor chip package manufacturing method.
USE - For electronic device, information apparatus, etc.
ADVANTAGE - Simplifies mounting of chip by etching plate selectively corresponding to conductivity pattern. DESCRIPTION OF DRAWING(S) - The figure shows partially notched perspective diagram of semiconductor chip package. (3) Adhesive **layer**; (5) Bonding **wire**; (7) Sealing portion; (12) Penetration **hole**.
Dwg.1/14

AB KR 99085107 A UPAB: 20010628
NOVELTY - A semiconductor chip and insulating plate with a penetration **hole** (12) are bonded together by adhesive agent (3). A conductive pattern is formed on the lower surface of the insulating plate so that the wire bonding is exposed in the **hole**. A bonding wire (5) connects a bonding pad and the **conductive** pattern, **electrically**
. DETAILED DESCRIPTION - A sealing portion (7) seals the semiconductor chip in order to protect from external environment. An INDEPENDENT CLAIM is also included for semiconductor chip package manufacturing method.
USE - For electronic device, information apparatus, etc.
ADVANTAGE - Simplifies mounting of chip by etching plate selectively corresponding to conductivity pattern. DESCRIPTION OF DRAWING(S) - The figure shows partially notched perspective diagram of semiconductor chip package. (3) Adhesive **layer**; (5) Bonding **wire**; (7) Sealing portion; (12) Penetration **hole**.
Dwg.1/14

L19 ANSWER 8 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-649329 [63] WPIX
DNN N2000-481446 DNC C2000-196490
TI High density wiring member manufacture for semiconductor chip mounting board, involves forming pattern shaped resist **image** on through **hole** circumference and etching metal layer on which resist **image** is not formed.
DC L03 U11 U14 V04
PA (HITB) HITACHI CHEM CO LTD
CYC 1
PI JP 2000165018 A 20000616 (200063)* 4p
ADT JP 2000165018 A JP 1998-332103 19981124
PRAI JP 1998-332103 19981124
AB JP2000165018 A UPAB: 20001205
NOVELTY - A photosensitive resist layer is formed on metal layer except on formation area of via **hole** (3). Resist **images** A and B are formed on circumference and interior of **hole**, respectively. The resist **images** A, B are removed by half etching of metal **layer**. Then **wiring** pattern shaped resist **image** C is formed on the circumference of through **hole** in metal layer and area other than that on metal layer are etched.
DETAILED DESCRIPTION - The through **hole** is formed on a metal layer formed on the insulating layer.
USE - For testing **electrical** property and **conduction** resistance property of boards such as printed circuit board, liquid crystal display board, integrated circuit board for semiconductor chip mounting board, flip-chip mounting board.
ADVANTAGE - Improves the positioning accuracy of bump in guide **hole**.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view explaining the resist lamination process on metal layer.
Through **hole** 3
Dwg.3/10

L19 ANSWER 9 OF 41 WPIX (C) 2002 THOMSON DERWENT

AN 2000-632132 [61] WPIX
CR 2001-070898 [08]
DNN N2000-468381 DNC C2000-190632
TI Multilayer board with tape automated bonding tape, chip size package, ball grid array tape, has through-**holes** filled with conductor by punching press and **wiring layers** connected **electrically** to **conductors**.
DC A85 L03 U11 V04
PA (MITG) MITSUI MINING & SMELTING CO LTD; (MITG) MITSUI KINZOKU KOGYO KK; (MITG) MITSUI MINING & SMELTING CO; (SUZM) SUZUKI CO LTD
CYC 3
PI JP 2000243791 A 20000908 (200061)* 5p <--
KR 2000062593 A 20001025 (200124)
TW 459316 A 20011011 (200247) <--
ADT JP 2000243791 A JP 1999-43868 19990222; KR 2000062593 A KR 2000-8499 20000222; TW 459316 A TW 2000-103054 20000222
PRAI JP 1999-43868 19990222; JP 1999-144275 19990525
AB JP2000243791 A UPAB: 20020725
NOVELTY - **Wiring layers** (2) are provided on both sides of a polyimide insulating substrate (1) which has through-**holes** formed by punching press. The through-**holes** are filled with conductor (3) by punching press. The conductor and **wiring layers** are connected electrically.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the multilayer board manufacturing method.
USE - Multilayer board with tape automated bonding (TAB) tape, chip size package (CSP) and ball grid array (BGA) tape.
ADVANTAGE - Reliability of electric connection between the conductor and **wiring layers** is improved. The process is extremely simple and so cost reduction is achieved. Since dry type multilayer board is manufactured, recycle of waste liquid is possible. So outstanding construction method with environmental preservation is obtained.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic sectional view of through-**hole** multilayer board.
Insulating substrate 1
Wiring layers 2
Conductor 3
Dwg.2/7

L19 ANSWER 10 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 2000-152939 [14] WPIX
DNN N2000-113922
TI Electrical connection between **wiring layer** terminal and chip electrode pad for semiconductor device.
DC U11
PA (NIDE) NEC CORP
CYC 1
PI JP 2000012626 A 20000114 (200014)* 5p <--
ADT JP 2000012626 A JP 1998-177828 19980624
PRAI JP 1998-177828 19980624
AB JP2000012626 A UPAB: 20000320
NOVELTY - The position on which the terminal section (3a) of a **wiring layer** (3) is formed is made to correspond to a carrier film (1). A through **hole** (12) is formed on the same position on which the terminal section of the **wiring layer** is formed. A chip electrode pad (10) is arranged to a semiconductor chip (9). An anisotropic conductivity film (4) includes an **electrically conductive** particle (4a).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a semiconductor device manufacture.

USE - For semiconductor device.

ADVANTAGE - Increases productivity of the junction since parallelism adjustment does not need to be performed. Reduces manufacturing cost since the metal bump does not need to be formed.

DESCRIPTION OF DRAWING(S) - The figures show the top view (a) and the sectional (b) of the semiconductor device.

Carrier film 1

Wiring layer 3

Terminal section 3a

Anisotropic conductivity film 4

Electrically conductive particle 4a

Semiconductor chip 9

Chip electrode pad 10

Through **hole** 12

Dwg.1/3

L19 ANSWER 11 OF 41 WPIX (C) 2002 THOMSON DERWENT

AN 1999-504440 [42] WPIX

DNN N1999-377248 DNC C1999-147830

TI Multilayer wiring board in semiconductor device for mounting semiconductor chips - has upper insulating layer contacting most external **wiring layer** of board, whose elasticity is lesser than that of lower insulating **layer** contacting **wiring layer** below external **wiring layer.**

DC A14 A21 A85 L03 U14 V04

PA (HITB) HITACHI CHEM CO LTD

CYC 1

PI JP 11219978 A 19990810 (199942)* 5p <--

ADT JP 11219978 A JP 1998-20103 19980202

PRAI JP 1998-20103 19980202

AB JP 11219978 A UPAB: 19991103

NOVELTY - The multilayer wiring board has a **conducting hole** to **electrically** connect the **wiring layers**. The elasticity of an upper insulating layer touching most external **wiring layer** is lesser than that of lower insulating **layer** touching a **wiring layer** below the external **wiring layer.**

DETAILED DESCRIPTION - The wiring board has a terminal (B) arranged opposite to a terminal (A) of a semiconductor chip. The semiconductor chip is mounted on the board by carrying out heat pressure application of an adhesive between the terminal of the chip and the terminal of the board. The storage modulus of the upper insulating layer measured using a dynamic visco-elasticity measuring apparatus is 2-20 Mpa at 25 deg. C and is 4-400 Mpa at 170 deg. C. The storage modulus of the lower insulating layer is 4-15 Mpa at 25 deg. C and is more than 1000 Mpa at 170 deg. C. The adhesive has an epoxy resin, an acrylic rubber which has a glycidyl ether group, a hardener and 0.1-20 volume % of an **electrically conductive** particle. The semiconductor device has the semiconductor chip as the electronic component.

USE - For mounting semiconductor chip in semiconductor device.

ADVANTAGE - The semiconductor device with excellent connection dependability of the semiconductor chip and the wiring board is obtained. The connection dependability improves sharply because there is no short circuiting in the inner circuit of the wiring board during the bias (100V) test even under conditions of high temperature and high humidity. Since electrode of the chip is embedded in the board after connection of the terminals ensuring that there is no unevenness between the semiconductor chip and the board, and since the thickness of the lower insulating layer which has higher modulus is secured, the connection dependability of the board is improved sharply.

Dwg.0/0

L19 ANSWER 12 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1999-450130 [38] WPIX
DNN N1999-336611 DNC C1999-132411
TI Solder bump formation for use during semiconductor device manufacture - by removing area other than connection **hole** area of **electrically conductive** films and forming solder bump above upper **electrically conductive** film.
DC L03 U11
PA (NIDE) NEC CORP
CYC 1
PI JP 11186308 A 19990709 (199938)* 8p <--
ADT JP 11186308 A JP 1997-351124 19971219
PRAI JP 1997-351124 19971219
AB JP 11186308 A UPAB: 19990922
NOVELTY - An **electrically conductive** film (106) containing nitrogen is formed above an insulating film (104), above which a further **electrically conductive** film (107a) is formed. The area other than connection **hole** area of the **electrically conductive** films (106a, 107a) is removed and a solder bump (109) is formed above the **electrically conductive** film (107a).
DETAILED DESCRIPTION - A wiring electrode (103) is formed on an insulating film (102), on a semiconductor substrate (101). A further insulating film (104) is formed above the wiring electrode. A connection **hole** is formed on the insulating film (104) to expose wiring electrode.
USE - For use during semiconductor device manufacture.
ADVANTAGE - Mechanical strength and electrical property of the solder bump are not degraded even when the thickness of **electrically conductive** films are small. Simplifies formation of slider bump with favourable electrical property and high reliability.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the process involved in semiconductor device manufacture. (102,104) Insulating **films**; (103) **Wiring** electrode; (106a,107a) **Electrically conductive** films; (109) Solder bump.
Dwg.4/17

L19 ANSWER 13 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1999-250587 [21] WPIX
DNN N1999-187198
TI Organic EL display device for domestic electrical appliances - arranges **electrically conductive** layer and insulating layer alternately in connector provided between organic EL display and wiring board.
DC P85 U14 X26
PA (DENK) TDK CORP
CYC 1
PI JP 11074075 A 19990316 (199921)* 8p
ADT JP 11074075 A JP 1997-275172 19970922
PRAI JP 1997-178863 19970619
AB JP 11074075 A UPAB: 19990603
NOVELTY - An **electrically conductive** layer (31) whose allowable current density is atleast 50mA divided by mm2, and an insulating layer (32) are arranged alternately in elastic connector (3).
DETAILED DESCRIPTION - A simple matrix type or segment mold type or simple matrix segment mixture type organic EL display (1) has an organic EL layer between cathode and **hole** injection electrode of light emitters.
An elastic connector (3) is provided between the leadout electrode of the display and the electrode of a wiring board (2).
USE - For domestic electrical appliances, measuring instrument panel

of motor vehicles, moving **image** and still picture display etc.
ADVANTAGE - As the display device is compact and thin, manufacture of display device is simplified and made inexpensive. Also space required for mounting display device is reduced. As the allowable current density of the **electrically conductive** layer of the connector is atleast 50mA divided by mm2, leakage current is prevented, thus non-uniformity in brightness is prevented to exhibit high quality display. DESCRIPTION OF DRAWING(S) - The figure shows the conceptual diagram showing the basic structure of the organic EL display device. (1) Organic EL display; (2) **Wiring** board; (3) **Elastic** connector; (31)**Electrically conductive** layer; (32) Insulating layer.
Dwg.1/9

L19 ANSWER 14 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1999-177543 [15] WPIX
DNN N1999-131057
TI BGA type semiconductor device - has metal bumps that are formed on land provided at back side of PCB.
DC U11 V04
PA (NIDE) NEC CORP
CYC 1
PI JP 11031713 A 19990202 (199915)* 6p <--
JP 3024596 B2 20000321 (200019) 5p <--
ADT JP 11031713 A JP 1997-184759 19970710; JP 3024596 B2 JP 1997-184759 19970710
FDT JP 3024596 B2 Previous Publ. JP 11031713
PRAI JP 1997-184759 19970710
AB JP 11031713 A UPAB: 19990416
NOVELTY - An IC chip (13) has a **hole** formed internally, through which the chip connection lead (4) is electrically connected. Metal bumps (10) are formed on lead provided at rear side of PCB. DETAILED DESCRIPTION - A metallic foil wiring is formed on the surface of a PCB (5). An IC chip connection lead is formed on a film carrier tape (1) using the metal **wiring**. A ground **layer** (6) is formed on the PCB. The IC chip connection lead in the film carrier tape is attached to the IC chip formed on the PCB using an anisotropic **electrically conductive** adhesive agent (11).
USE - None given.
ADVANTAGE - The IC chip is mounted easily. Inductance is reduced by ground layer in the PCB. DESCRIPTION OF DRAWING(S) - The figure shows sectional drawing of BGA type semiconductor device. (1) Film carrier tape; (4) IC chip connection lead; (5) PCB; (6) Ground layer; (10) Metal bumps; (11) Anisotropic **electrically conductive** adhesive agent; (13) IC chip.
Dwg.1/4

L19 ANSWER 15 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1999-127544 [11] WPIX
DNN N1999-093724
TI HF chip carrier for semiconductor light control element - has ground layer provided in lower surface of HF substrate, connected electrically with intermediate ground layer via through **hole**.
DC P81 U11 W02
PA (OKID) OKI ELECTRIC IND CO LTD
CYC 1
PI JP 11003904 A 19990106 (199911)* 14p <--
ADT JP 11003904 A JP 1997-155595 19970612
PRAI JP 1997-155595 19970612
AB JP 11003904 A UPAB: 19990316
NOVELTY - A HF electrical wiring substrate (12) provided in carrier base

(14) has several electric insulating layer (28) and HF electrical wirings (18,20). A taper section (16) is provided in the HF substrate. An intermediate ground layer is arranged on the surface of the electrical insulating layer in parallel with the electrical **wiring**. A ground **layer** provided in the substrate **conducts electrically** with the intermediate layer via a through **hole**.

USE - For semiconductor light control element.

ADVANTAGE - The value of characteristic impedance is not reduced. The scattering of unnecessary light is prevented. DESCRIPTION OF DRAWING(S) - The figure shows the plan and side view of chip carrier. (12) Wiring substrate; (14) Carrier base; (16) Taper section; (18,20) HF electrical wirings; (28) Electric insulating layer.

Dwg.1/10

L19 ANSWER 16 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1998-339336 [30] WPIX
DNN N1998-265540
TI Tape carrier package for electronic device - includes through-**hole** by which conductive electrode and metal **wiring layer** are connected electrically.
DC U11
PA (NIDE) NEC CORP
CYC 1
PI JP 10125721 A 19980515 (199830)* 7p <--
ADT JP 10125721 A JP 1996-274728 19961017
PRAI JP 1996-274728 19961017
AB JP 10125721 A UPAB: 19980730

The package includes an insulating tape (15) on which a metal **wiring layer** (14) is formed on both sides. A semiconductor chip (1) is mounted on the insulating tape. The electrode of semiconductor chip is connected to the **wiring layer** of the insulating tape. An **electrically conductive** protrusion as external connecting terminal and a conductive electrode are provided on the back side of the insulating tape.

A through-**hole** (5) is provided to connect **electrically** the **conductive** electrode provided on the back side of the tape insulating film, with the metal **wiring layer**. A ground plane layer (10) is provided for the power supply on the one side of the insulating tape.

ADVANTAGE - Prevents reduction of electrical property. Attains wiring area enlargement. Minimizes wiring length extremely. Simplifies wiring pattern. Avoids influence by layout of electrode pin and ground pin. Offers miniaturized tape carrier package.

Dwg.1/8

L19 ANSWER 17 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1997-556775 [51] WPIX
DNN N1997-464063
TI Pad electrode structure for semiconductor device - has pair of **wiring films** electrically connected by connection **hole** in interlayer insulating film.
DC U11
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 09270426 A 19971014 (199751)* 4p
ADT JP 09270426 A JP 1996-77658 19960329
PRAI JP 1996-77658 19960329
AB JP 09270426 A UPAB: 19971222

The structure includes a pair of **electrically conductive wiring films** (102,104), electrically connected through a

connection **hole** formed in an interlayer insulating film (103).
The connection **hole** has side wall parts formed in it.
ADVANTAGE - Improves manufacturing efficiency and reliability of interlayer insulating film.
Dwg.2/3

L19 ANSWER 18 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1997-408668 [38] WPIX
DNN N1997-340085
TI Semiconductor device wiring method - involves forming upper **wiring layer** such that it is coupled with **electrically conductive** layer formed in contact **hole** on lower **wiring layer.**
DC U11
IN CHON, Y; JEON, Y G; Y, K
PA (GLDS) GOLDSTAR ELECTRON CO LTD; (HYUN-N) HYUNDAI MICROELECTRONICS CO LTD; (GLDS) LG SEMICON CO LTD
CYC 3
PI JP 09181178 A 19970711 (199738)* 7p
US 5837604 A 19981117 (199902)
KR 97052291 A 19970729 (199910)
JP 3072544 B2 20000731 (200041) 6p
KR 172851 B1 19990330 (200045)
ADT JP 09181178 A JP 1996-177184 19960619; US 5837604 A US 1996-698699 19960816; KR 97052291 A KR 1995-52205 19951219; JP 3072544 B2 JP 1996-177184 19960619; KR 172851 B1 KR 1995-52205 19951219
FDT JP 3072544 B2 Previous Publ. JP 09181178
PRAI KR 1995-52205 19951219
AB JP 09181178 A UPAB: 19970922
The method involves forming a contact **hole** to a lower **wiring layer** (2) which is covered by a Si oxide film (3) on a semiconductor substrate (1). An **electrically conductive** layer (6) is formed in this contact **hole.**
An upper **wiring layer** (6a) is formed on the contact **hole** such that it contacts **electrically conductive** layer. Thus, the lower and upper **wiring layers** are connected through the **electrically conductive** layer.
ADVANTAGE - Prevents boundary surface of upper and lower **wiring layers,** being contaminated by impurities. Improves reliability and contact resistance. Simplifies wiring process. Improves wiring characteristics.
Dwg.1/4

L19 ANSWER 19 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1996-293134 [30] WPIX
DNN N1996-246409 DNC C1996-093423
TI Semiconductor device mfg. method - by making second layer recess adhere to **electrically conductive** film to connect it to the first layer through a **hole**..
DC L03 U11
PA (NIDE) NEC CORP
CYC 1
PI JP 08124927 A 19960517 (199630)* 7p
ADT JP 08124927 A JP 1994-265567 19941028
PRAI JP 1994-265567 19941028
AB JP 08124927 A UPAB: 19960731
Mfr. involves forming a semiconductor element on a substrate (101). A bonding pad (109), a first **wiring layer** (104) and an insulating film (102) are formed at the main field of the substrate. The spacer of an insulating material is formed at the first area of the first

insulating film and a first **wiring layer** is formed on the second area of the first insulating film. A second flat insulating film covers the spacer, the first **wiring layer** and the first area.

A recess is formed by etching the second insulating film selectively thereby exposing the first insulating film and boundary positions of the upper face of the spacer. A bonding pad is also formed. The recess of the second layer is adhered to an **electrically conductive** film and is connected to the first layer through a through **hole**. The spacer is formed at the open **hole** part of the interlayer insulating film by the CVD oxide film.

ADVANTAGE - Reduces thickness of interlayer insulating film. High mfg. yield results. Enables removal of wiring material of second layer completely.

Dwg.1/3

L19 ANSWER 20 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1996-265800 [27] WPIX
DNN N1996-223556
TI **Wiring film** for tape automated bonding - has wiring pattern of **electrically conductive** metal used in electric connected to one surface of film.
DC U11
PA (ADVA-N) ADVANTEST KK
CYC 1
PI JP 08111435 A 19960430 (199627)* 5p <--
ADT JP 08111435 A JP 1994-268232 19941006
PRAI JP 1994-268232 19941006
AB JP 08111435 A UPAB: 19960710
The film has an electric insulation (1) with a mechanical curvature quality. An electric connection is made between a wiring pattern (2), the wiring position of a bare-chip IC (3), and a node (6) by the side of a wiring board (4) to eliminate film **hole** (5) formation.

The **film** forms a **wiring** pattern of the **electrically conductive** metal used in electric connection to one surface of the film.

ADVANTAGE - Improves frequency characteristics in high peripheral wave-band region. Expands surface area and cross-sectional area of wire of tape automated bonding compared to wire of chip-on-bonding.

Dwg.2/9

L19 ANSWER 21 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1995-160481 [21] WPIX
CR 1994-279011 [34]
DNN N1995-125866
TI Semiconductor circuit assembly construction method for chip carrier in flip-chip mounting - applying conductive coatings to both sides of substrate, forming conductive pads corresp. to die bond pads and for connection to printed **wiring** board, with **coatings** extending into shaped through-**holes**.
DC U11 U14
IN BRICE-HEAMES, K; FREI, J K
PA (MOTI) MOTOROLA INC
CYC 1
PI US 5401689 A 19950328 (199521)* 16p <--
ADT US 5401689 A Div ex US 1992-994380 19921221, US 1994-210486 19940422
FDT US 5401689 A Div ex US 5342999
PRAI US 1992-994380 19921221; US 1994-210486 19940422
AB US 5401689 A UPAB: 19950602
The semiconductor die carrier formation, for a die having N bond pads, involves a) forming a substrate (30) with N **holes** (26) extending

between two sides, the **holes** having a smaller dia. in a central portion compared with outer portions; b) applying a conductive coating (48) to one side (40) of the substrate, the coating extending onto substrate protrusions within the **holes** (28a, 28b) and onto the substrate side to provide N **conductive** pads (53) **electrically** coupled to the corresp. **holes**; and c) applying a second conductive coating (58) to the other side of the substrate (42), extending onto substrate protrusions within the **holes** for N additional conductive pads coupled to corresp. **holes**.

Pref. the bond pads are overlaid with a conductive bump formed of Au alloy with a Pt-group metal and are welded to one set of corresp. pads by thermal compression. Solder bumps are formed on the second set of pads and used to bond these pads to a printed wiring board.

ADVANTAGE - Compatible with existing testing facilities; inexpensive, suitable for small prodn. runs.

Dwg.10/19

L19 ANSWER 22 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1995-108164 [15] WPIX
DNN N1995-085522
TI Multi-chip module e.g. in PGA package - includes thin film multilayer circuit board on substrate surface, facing mounting circuit board, and on which terminals and LSIs are attached to pads, with wiring conductors and insulating layers.
DC U11 U14
IN HIRANO, M; KIKUCHI, S; NORI, H; SEYAMA, K; SUMIYOSHI, M; YASUDA, N
PA (FUIT) FUJITSU LTD
CYC 5
PI EP 638931 A2 19950215 (199515)* EN 14p
R: DE FR GB
JP 07058276 A 19950303 (199518) 8p
EP 638931 A3 19950510 (199546)
US 5586006 A 19961217 (199705) 13p
JP 3110922 B2 20001120 (200101) 8p
ADT EP 638931 A2 EP 1994-400928 19940429; JP 07058276 A JP 1993-200736 19930812; EP 638931 A3 EP 1994-400928 19940429; US 5586006 A Cont of US 1994-234880 19940428, US 1995-573577 19951215; JP 3110922 B2 JP 1993-200736 19930812
FDT JP 3110922 B2 Previous Publ. JP 07058276
PRAI JP 1993-200736 19930812
AB EP 638931 A UPAB: 19950425
The MCM includes a thin film multilayer circuit board (32), with insulating **layers** and **wiring** conductors, on a substrate surface. There are circuit elements mounted on the multilayer circuit surface. Terminals (34) attached to the thin film multilayer circuit board surface electrically connect the wiring conductors to circuits on a wiring board on the which the module is mounted.

Ther terminals may be leads or leadless, with the leads being e.g. vertical lead pins, flat lead pins, wire leads to tape-automated bonding leads. Pref. the terminals are soldered to wiring conductors facing the mounting wiring board, with the terminals supported by the thin film multilayer circuit board. The terminals are pref. connected to pads on the multilayer circuit board.

USE/ADVANTAGE - Allows cooling structure attachment. Avoids wiring conductors in substrate; **flexible wiring** design and module shape.

Dwg.5/15

L19 ANSWER 23 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1995-058111 [08] WPIX

DNN N1995-045987
TI Semiconductor device mounting method - involving formation of through **hole** and connection of **electrically conductive** layer and **electrically conductive** electrode.
DC U11
PA (NIEM) NIPPON CHEMICON CORP
CYC 1
PI JP 06338539 A 19941206 (199508)* 5p <--
ADT JP 06338539 A JP 1993-151542 19930528
PRAI JP 1993-151542 19930528
AB JP 06338539 A UPAB: 19950301
The mounting method involves using a wiring board (3) which is formed by layering an **electrically conductive** layer (2) on an insulating **film** (1). The **wiring** board possesses the wiring pattern. An IC chip (4) having electrodes (5) is directly mounted on the wiring board. The through **hole** (6) formed in the **electrically conductive** layer and insulation film meets the electrode.

After carrying out position matching of electrode and through **hole**, a conductive material member (7) is filled into the through **hole**. Thus, the **electrically conductive** layer and **electrically conductive** electrode are connected.

ADVANTAGE - Narrows wiring pitch of wiring pattern. Increases number of output terminals. Reduces area of mounting portion thereby reducing occupancy capacitance of element. Reduces manufacturing cost.
Dwg.1/4

L19 ANSWER 24 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1995-058110 [08] WPIX
DNN N1995-045986
TI Connection method of semiconductor element - involving formation of through **hole, electrically conductive** layer and **electrically conductive** electrode which are connected electrically.
DC U11
PA (NIEM) NIPPON CHEMICON CORP
CYC 1
PI JP 06338538 A 19941206 (199508)* 4p <--
ADT JP 06338538 A JP 1993-151541 19930528
PRAI JP 1993-151541 19930528
AB JP 06338538 A UPAB: 19950301
The method makes use of a wiring board (3) which is formed by layering an **electrically conductive** layer (2) on an insulating **film** (1). The **wiring** board has wiring pattern deposited on it. An IC chip (4) having electrodes (5) over it is adhered to the rear side of the wiring board by means of an adhesive agent (9).

A through **hole** (6) formed in the **electrically conductive** layer and the insulation film contacts the electrode. Then, an **electrically conductive** layer (7) is formed in the through **hole**. Thus, the **electrically conductive** layer and the **electrically conductive** electrode are connected electrically.

ADVANTAGE - Narrows wiring pitch of wiring pattern. Reduces area of mounting portion, thereby reducing spurious capacitance of element. Increases number of output terminals. Mounts semiconductor element efficiently.
Dwg.1/4

L19 ANSWER 25 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1995-055630 [08] WPIX
DNN N1995-043819 DNC C1995-025276

TI Semiconductor device high resolution electrode manufacturing method for flip chip IC - involves forming electric conduction film layer in contact **hole** pedestal which is subsequently etched to exact diameter of pillar shaped solder plated copper electrode super structure.
DC L03 U11
PA (NPDE) NIPPONDENSO CO LTD
CYC 1
PI JP 06333931 A 19941202 (199508)* 8p
ADT JP 06333931 A JP 1993-118585 19930520
PRAI JP 1993-118585 19930520
AB JP 06333931 A UPAB: 19950301
The semiconductor device high resolution electrode manufacturing method is applied to a semiconductor element. Passivation film (14) is formed on the Al **wiring layer** (13) according to whole pattern.
Earlier the Al **wiring layer** is formed on a semiconductor substrate (11). Then **electrical conductive** layer (16) is formed on the passivation film. A resist film (17) is applied on **electrically conducting** layer and its exposed by photolithographic process. Then photo **hole** (18) is formed by removing unhardened resist.
A copper plating (19) and solder plating (20) are applied in the photo **hole** followed by reflow solder plating to generate a pillar shaped electrode. Then the hardened resist is removed. The device is then processed in RIE apparatus in gas plasma containing oxygen radical, the execute anisotropic etching. The acceleration impulse is generated in the process through electric field. The etching process removes the exposed portion of **electrical conductive** layer (16), trimming the pillar shaped electrode base.
ADVANTAGE - Rationalises photo **hole** shape. Provides convex electromotive pole with high integration density without constriction in lower part of photo **hole**. Equalises diameter of electrode in upper part and lower part.
Dwg.1/10

L19 ANSWER 26 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1995-026167 [04] WPIX
DNN N1995-020533 DNC C1995-012023
TI High frequency variable capacitance diode bonding method - involves forming electroconducting film over insulating **film** and forming **wire** bond over substrate.
DC L03 U11 U12
PA (TOJK) TOKO KK
CYC 1
PI JP 06310560 A 19941104 (199504)* 4p <--
ADT JP 06310560 A JP 1993-120603 19930423
PRAI JP 1993-120603 19930423
AB JP 06310560 A UPAB: 19950201
The variable capacitance diode (10) has P-N junction which is formed parallel to the surface of the substrate. An insulation film (11) is formed over the substrate leaving open **holes** for electrical contact.
An **electrically conducting** film (12) is formed over the insulation film to form domain for contact of inspection needle and bonding pad for wire bonding on the substrate. A wire bonding (13) is performed over the layer.
ADVANTAGE - Puncture of P-N junction during inspection. Maintains constant area of element. Increases yield and reliability. Prevents generation of floating capacitance.
Dwg.1/4

L19 ANSWER 27 OF 41 WPIX (C) 2002 THOMSON DERWENT

AN 1993-267897 [34] WPIX
DNN N1996-064623
TI Wiring conductor holding semiconductor device for high speed multi-processor computer - has substrate with perpendicular through **holes** filled with conductive material with conductive pins inserted at one side contacting **wiring layer** at other.
DC U11 U14 V04
IN FUJITA, Y; MIZUISHI, K
PA (HITA) HITACHI LTD
CYC 3
PI JP 05183019 A 19930723 (199334)* 8p <--
US 5485039 A 19960116 (199609)B 14p
KR 139276 B1 19980601 (200015) <--
ADT JP 05183019 A JP 1991-345833 19911227; US 5485039 A US 1992-990029 19921214; KR 139276 B1 KR 1992-25179 19921223
PRAI JP 1991-345833 19911227
AB US 5485039 A UPAB: 19960305 ABEQ treated as Basic
The device includes a semiconductor substrate, several wiring conductors, buried **conductive** material, and **electrically conductive** pins. The substrate has several through **holes** extending through it which are perpendicular to its two main surfaces. The wiring conductors are provided at one the substrate surfaces.
The **electrically conductive** material is buried into each of the through **holes** and is connected to at least one of the wiring conductors. The pins are each provided at substrate surface opposite the wiring surface corresponding to a through **hole**. Each pin is electrically connected to the material buried into its respective through **hole**. A portion of the pin extends from the pin providing surface to the substrate outside. Each pin further has a portion inserted into the material buried into the through **hole** at which it is located.
USE/ADVANTAGE - Also for LSI, high density three dimensional layer. Has several high accuracy through **holes**. Has increased reliability.
Dwg.1/16
AB JP 05183019 A UPAB: 20000323
The device includes a semiconductor substrate, several wiring conductors, buried **conductive** material, and **electrically conductive** pins. The substrate has several through **holes** extending through it which are perpendicular to its two main surfaces. The wiring conductors are provided at one the substrate surfaces.
The **electrically conductive** material is buried into each of the through **holes** and is connected to at least one of the wiring conductors. The pins are each provided at substrate surface opposite the wiring surface corresponding to a through **hole**. Each pin is electrically connected to the material buried into its respective through **hole**. A portion of the pin extends from the pin providing surface to the substrate outside. Each pin further has a portion inserted into the material buried into the through **hole** at which it is located.
USE/ADVANTAGE - Also for LSI, high density three dimensional layer. Has several high accuracy through **holes**. Has increased reliability.
Dwg.1/15

L19 ANSWER 28 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1993-258927 [32] WPIX
DNN N1993-199173
TI **Flexible** multilayer circuit **wiring** board - has circuit conductors forming finger lead-like terminals made of material with high Young's modulus, and **flexible wiring** conductors on

other side of insulating base.
DC U11
IN INABA, M; IWAYAMA, T; MIYAGAWA, A
PA (NIMF) NIPPON MEKTRON KK
CYC 3
PI WO 9315520 A1 19930805 (199332)* JA 10p <--
W: DE US
JP 05206589 A 19930813 (199337)
US 5408052 A 19950418 (199521) 5p
JP 3330387 B2 20020930 (200271) 3p
ADT WO 9315520 A1 WO 1993-JP29 19930112; JP 05206589 A JP 1992-34489 19920124; US 5408052 A WO 1993-JP29 19930112, US 1993-117150 19930913; JP 3330387 B2 JP 1992-34489 19920124
FDT US 5408052 A Based on WO 9315520; JP 3330387 B2 Previous Publ. JP 05206589
PRAI JP 1992-34489 19920124
AB WO 9315520 A UPAB: 19931118
The **flexible** multilayer circuit **wiring** board has, on one end of one side of a flexible insulation base material (1), circuit conductors (2) which are for forming finger lead-like terminals (3), and made of a conductive metal having a high Young's modulus.

On the other side of the flexible insulation base material (1) inclusive of a bent part (A) of the circuit wiring board, provided is a required circuit wiring conductor (4) made of a conductive metal having a high flexibility. A through-**hole** (5) is provided by which the circuit conductors (2) and the required parts of the circuit **conductor** (4) are **electrically** connected to each other.

ADVANTAGE - Finger-like terminals are hard to deform even when forming finer circuit conductors protruded in form of finger leads whose bent part is sufficiently flexible.
Dwg.1/3

L19 ANSWER 29 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1991-009089 [02] WPIX
DNN N1991-007133
TI Pin grid array packaged semiconductor device - carries multi-level interconnection structure for connecting device by thermocompression bonding.
DC U11
IN HARADA, S; MATSUKI, H; SUGIMOTO, M; YOSHIDA, T
PA (FUIT) FUJITSU LTD; (FUIV) FUJITSU VLSI LTD
CYC 6
PI EP 405755 A 19910102 (199102)*
R: DE FR GB
JP 03072644 A 19910327 (199119)
US 5065223 A 19911112 (199148)
EP 405755 A3 19920826 (199337)
KR 9310074 B1 19931014 (199438)
EP 405755 B1 19951129 (199601) EN 19p
R: DE FR GB
DE 69023819 E 19960111 (199607)
ADT EP 405755 A EP 1990-305893 19900530; JP 03072644 A JP 1990-142185 19900531; US 5065223 A US 1990-531457 19900531; EP 405755 A3 EP 1990-305893 19900530; KR 9310074 B1 KR 1990-8049 19900531; EP 405755 B1 EP 1990-305893 19900530; DE 69023819 E DE 1990-623819 19900530, EP 1990-305893 19900530
FDT DE 69023819 E Based on EP 405755
PRAI JP 1989-137889 19890531
AB EP 405755 A UPAB: 19931123
The semiconductor chip (21) is mounted on an aluminium nitride substrate (22). About one hundred of lead wires each having a cross sectional area of 1200 square micrometre, are provided on each edge of the chip. The

nickel coated 0.15 mm diameter `Kovar' (RTM) connection pins (29 are arranged in rows and columns to form the pin grid array.

The device is hermetically sealed by the aluminium nitride heat sink (33) and the `Kovar' (RTM) Cap (34). A peripheral metallisation (220) is provided on the substrate to obtain an excellent connection with the cap.

ADVANTAGE - Optimised configuration leading to multi-level package. Increased number of connection pins. @(15pp Dwg.No.5/13)@
5/13

L19 ANSWER 30 OF 41 WPIX (C) 2002 THOMSON DERWENT
AN 1982-M0698E [37] WPIX
TI High density connections between semiconductor and circuit board - has **flexible wiring** membrane attached to bottom of substrate, provided with electrical contacts to be mated to complementary contacts in PCB.
DC U11 U14 V04
IN ECKER, M E; OLSON, L T
PA (IBMC) IBM CORP
CYC 5
PI EP 59337 A 19820908 (198237)* EN 45p
R: DE FR GB
JP 57155751 A 19820925 (198244)
US 4377316 A 19830322 (198314)
EP 59337 B 19860813 (198633) EN
R: DE FR GB
DE 3272501 G 19860918 (198639)
ADT EP 59337 A EP 1982-100843 19820205
PRAI US 1981-238873 19810227
AB EP 59337 A UPAB: 19930915
A semiconductor chip (70), carried on a substrate (11) is mounted on a printed circuit board by a **flexible**, extendable **wiring** membrane (50) attached to the bottom of and extending beyond the substrate. Contacts (51) are provided on the membrane beyond the periphery of the substrate. A conductive pattern is provided on the membrane between the chip and contacts. The chip and circuit board are maintained at a distance from each other by thermally and **electrically conducting** leaf springs. The membrane is pref. formed from a polyimide resin.

The membrane contacts (51) are pref. female contacts with male contacts provided on the printed circuit board. This obviates the requirement for completely plated through **holes**. Furthermore a large number of connections may be made to the semiconductor device by this method.
8/18

L19 ANSWER 31 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 2002-043373 JAPIO
TI FILM CARRIER AND MANUFACTURING METHOD THEREFOR
IN NAOI KOKUKO
PA TOPPAN PRINTING CO LTD
PI JP 2002043373 A 20020208 Heisei
AI JP 2000-226778 (JP2000226778 Heisei) 20000727
PRAI JP 2000-226778 20000727
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide a film carrier provided with an **electrically conductive** path with improved adhesion with electroplating and electric reliability accompanying the miniaturization of an **electrically conductive** path and the manufacturing method.
SOLUTION: In this film carrier, a first **wiring layer** is formed on one of the surfaces of an insulation **film**, a second

wiring layer including a plating layer is formed on the other surface, a via **hole** is closed by the first **wiring layer**, and the first **wiring layer** on the side of the insulation film of a via **hole** part is connected by the plating layer inside the via **hole** continued to the plating **layer**. The first **wiring layer** on the side of the insulation film of the via **hole** is etched by electrolytic etching and chemical etching.

L19 ANSWER 32 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 2001-345557 JAPIO
TI WIRING BOARD AND ELECTRONIC COMPONENT USING THE SAME
IN WAKASAKI AKIRA; KIRIKIHIRA ISAMU
PA KYOCERA CORP
PI JP 2001345557 A 20011214 Heisei
AI JP 2000-161385 (JP2000161385 Heisei) 20000531
PRAI JP 2000-161385 20000531
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To prevent wire breaking between a through **conductor**, which **electrically** connects the **wiring** conductor **layers** of a **wiring** board with each other, and the **wiring** conductor **layer**.
SOLUTION: This is a wiring board 6 which comprises an insulating substrate 1, a plurality of insulating layers 2 formed on the insulating substrate 1, **wiring** conductor **layers** 3 formed on each surface of the insulating substrate 1 and the plural insulating layers 2, and a through-**hole** 5 constituted of a conductor filled in the through-**hole** 4 bored from each surface of the plural insulating layer 2 to the rear and electrically connecting the **wiring** conductor **layers** 3 with one another. A stacked through- conductor part 10 is formed by arranging the conductor filled in the through-**hole** 4 of each insulating layer 2 in vertical direction, and also embedding the end on the rear side of the insulating layer 2 of each conductor to a depth of one-tenth to half the thickness of the **wiring** conductor **layer** in the **wiring** conductor **layer** 3 on the rear side of the insulating layer 2 on each conductor. This board can be made into a wiring board, which is high in reliability for connection without the occurrence of wire breaking, since the end on the rear side of the insulating layer 2 on each conductor is embedded in the **wiring** conductor **layer** 3 on the rear side of each insulating layer 2.

L19 ANSWER 33 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 2000-243791 JAPIO
TI TWO-METAL TAB AND DOUBLE-SIDED CSP, BGA TAPE, AND MANUFACTURE OF THEM
IN ICHIYANAGI AKIRA; TAKAHASHI MOTONOBU
PA MITSUI MINING & SMELTING CO LTD
PI JP 2000243791 A 20000908 Heisei
AI JP 1999-43868 (JP11043868 Heisei) 19990222
PRAI JP 1999-43868 19990222
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To enable a double-sided conductor layer to be improved in electrical connection reliability and lessened in manufacturing cost by a method, wherein a through-**hole** provided in the conductor layer is filled up with a conductor by a punching press to **electrically** connect the **conductor** with a **wiring layer**.
SOLUTION: Sprocket **holes** or through-**holes** are provided in a double-sided copper laminated polyimide tape by a press. Thereafter, the front of the copper laminated polyimide tape is surfaced, photoresist

is applied onto the polyimide tape, and a **wiring layer** is formed on the front surface of the copper laminated polyimide tape through exposure, development, and etching. Then, similarly, the rear of the copper laminated polyimide tape is surfaced, photoresist is applied onto the rear of the polyimide tape, and a **wiring layer** is formed on the rear surface of the copper laminated polyimide tape through exposure, development, and etching. In this process, through-**holes** are provided in the polyimide tape by a punching process, and the through-**holes** are filled with a conductor 3 by a punching press, by which the **conductor** 3 is **electrically** connected to the **wiring layer** 2 or a metal foil. The through-**hole** of a two-metal TAB is composed of an insulating board 1, a **wiring layer** 2, and the conductor 3.
COPYRIGHT: (C)2000,JPO

L19 ANSWER 34 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 2000-100878 JAPIO
TI MANUFACTURE OF DOUBLE-SIDED **WIRING FILM** CARRIER
IN ICHIYANAGI AKIRA; TAKAHASHI MOTONOBU
PA MITSUI MINING & SMELTING CO LTD
PI JP 2000100878 A 20000407 Heisei
AI JP 1998-266877 (JP10266877 Heisei) 19980921
PRAI JP 1998-266877 19980921
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide a manufacture of a double-sided **wiring film** carrier, having via **holes** which are filled with conductive paste and reliable conduction.
SOLUTION: In a manufacture of a double-sided **wiring film** carrier including an insulating base film, metal foils arranged on both surfaces of the film, one of the metal foils being a pattern layer and the other being a grounded flat layer, and via **holes** which are filled with **conductive** paste to **electrically** connect both layers, the via **holes** are filled with conductive paste from the front surface of the insulating film with the metal foil on the reverse surface with a screen printer. After the via **holes** are filled with conductive paste, the metal foil is heated and pressed on the insulating film to thermally cure the conductive paste.
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L19 ANSWER 35 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1999-340367 JAPIO
TI MULTILAYER WIRING BOARD AND ITS MANUFACTURE
IN HAYASHI KATSURA
PA KYOCERA CORP
PI JP 11340367 A 19991210 Heisei
AI JP 1998-149381 (JP10149381 Heisei) 19980529
PRAI JP 1998-149381 19980529
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a multilayer wiring board having various kinds of **wiring** circuit **layers** where fine circuit formation suitable for flip chip mounting is enabled, and connecting a member such as a connector, a metal fixture and a battery and applying a large current are enabled.
SOLUTION: A multilayer wiring board 1 is provided with an insulating board 2 which is formed by laminating insulating layers 2a-2d composed of insulating material containing at least thermosetting resin, **wiring** circuit **layers** formed on the surface and/or in the inside of the insulating substrate 2, and via **hole conductors** 4 for **electrically** connecting spaces between the **wiring** circuit **layers**. In the above multilayer wiring board 1, a plurality of **wiring** circuit **layers**

3a-3d which are constituted of metal foil or the like and have different thicknesses are formed in at least one of the insulating layers 2a-2d. At least **wiring** circuit **layers** 3a, 3b, 3c which are formed on the surface of the insulating substrate 2 out of the **wiring** circuit **layers** 3a-3d are buried in the surface of the insulating board 2. These sectional shapes are made almost reversely trapezoidal where edges of buried side are longer than those of exposed side.

L19 ANSWER 36 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1999-251374 JAPIO
TI DOUBLE FACE **WIRING FILM** CARRIER TAPE AND ITS MANUFACTURE
IN MASUKO YASUAKI
PA MITSUI MINING & SMELTING CO LTD
PI JP 11251374 A 19990917 Heisei
AI JP 1998-53985 (JP10053985 Heisei) 19980305
PRAI JP 1998-53985 19980305
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide fine wiring patterns on a surface and a back, by installing a plurality of connection **holes** for connecting the necessary parts of both faces of the patterns in an insulating film, filling the connection **holes** with **conductive** paste, and **electrically** connecting the wiring patterns of both faces.
SOLUTION: For manufacturing a double face **wiring film** carrier tape, copper foils 2a and 2b are adhered to both faces of an insulating film 1. Liquid photoresist is applied and copper foil on both faces is patterned so as to form wiring patterns 3a and 3b. Connection **holes** 4a being through **holes** and **holes** for positioning are formed in necessary parts. The connection **holes** 4a are filled with conductive paste 5 and the wiring patterns of both faces are electrically connected. Then, solder resist 6 is applied to the prescribed areas of the wiring patterns and the connection **holes** 4a filled with conductive paste so as to protect them. Thus, the double face wiring carrier tape where the fine wiring patterns of not more than 100 μm pitches exist on both faces can be mass-produced.

L19 ANSWER 37 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1999-219978 JAPIO
TI ELECTRONIC PART DEVICE
IN WATANABE ITSUO; TAKEMURA KENZO; TSURU YOSHIYUKI; URASAKI NAOYUKI; SHIMADA YASUSHI; NAKASO AKISHI
PA HITACHI CHEM CO LTD
PI JP 11219978 A 19990810 Heisei
AI JP 1998-20103 (JP10020103 Heisei) 19980202
PRAI JP 1998-20103 19980202
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide an electronic part device for a semiconductor device, etc., excellent in connection reliability between a mount board and an electronic part such as semiconductor chip, etc.
SOLUTION: The device comprises a plurality of **wiring layers** comprising an outer- most wring layer and a **conductive hole** for **electrically** connecting the **wiring layers**, and an insulating layer between the outer-most **wiring layer** and a **wiring layer** closest to it comprises a 2-layer insulating layer of different elastic modulus, and a semiconductor chip is mounted through a bonding agent to a mount board of a multi-layer interconnection wherein

the elastic modulus contacting to the outer-most **wiring layer** is smaller than that connecting to a **wiring layer** closest to the outer-most **wiring layer**. Thus, an electrode of the mount board is embedded in the board after connection for absorbing dispersion in height of semiconductor's bump and multi-layer substrate electrode, and the elastic modulus or the insulating layer connecting to a **wiring layer** closest to the outer-most **wiring layer** is larger than the outer-most **wiring layer** so that a thickness of an insulating layer connecting at least to a **wiring layer** closest to the outer-most **wiring layer** is assured, thus no short circuit with a substrate inner- layer circuit occurs for significantly improved connection reliability.

L19 ANSWER 38 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1999-045907 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN HAYASHI KATSURA
PA KYOCERA CORP
PI JP 11045907 A 19990216 Heisei
AI JP 1997-201652 (JP09201652 Heisei) 19970728
PRAI JP 1997-201652 19970728
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a semiconductor device and a manufacture thereof which can conveniently realize at a high productivity the mounting of semiconductor elements on a lead **wiring layer** formed on a multilayer wiring board having an insulation board made of an insulation material contg. an org. resin, and which is applicable to MCMs. SOLUTION: The semiconductor device having TAB-connected semiconductor elements is manufactured by TAB-connecting semiconductor elements 6 to a lead **wiring layer** 4 of a TAB tape 5 which is composed of a metal foil 3 formed on a transfer film 1, transferring the lead **wiring layer** 4 having the TAB-connected semiconductor elements 6 to the surface of an unhardened multilayer board 7 having a **wiring** circuit **layer** 10 and via-**hole conductors** 11 for **electrically** interconnecting the **wiring layers** on an insulation board 9 having laminated insulation layers contg. thermosetting resins, and heating it to perfectly harden the wiring board.

L19 ANSWER 39 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1997-008134 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN KAWAURA HISAO
PA NEC CORP
PI JP 09008134 A 19970110 Heisei
AI JP 1995-155815 (JP07155815 Heisei) 19950622
PRAI JP 1995-155815 19950622
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PURPOSE: To prevent a bonding pad from being peeled off by forming a second wiring with a metal film for laminating titanium nitride layer and aluminum alloy which are directly adhered to a second interlayer insulation film and the titanium film or aluminum alloy which is directly adhered to the second interlayer insulation film and titanium film. CONSTITUTION: A through **hole** 8 is formed on a second interlayer insulation film 7 for **electrical conduction** to a first-**layer wiring** 5'. Then, a through **hole** titanium film 9 is formed only on the first aluminum alloy 5 at the bottom of the through **hole** 8, thus forming third titanium nitride layer

10 and second aluminum alloy 11 and forming a bonding pad consisting of a second-**layer wiring** 11'. The through **hole** titanium film 9 is formed at the bottom of the through **hole** and no lead wire is formed at region to be bonded. Then, the third titanium nitride layer 10 is electrically connected to the first aluminum alloy 5 via the through **hole** titanium film 9 at the bottom of the through **hole** 8.
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L19 ANSWER 40 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1995-168532 JAPIO
TI ELECTRON RELEASING ELEMENT
IN HOSHINO AKIHIRO
PA TOPPAN PRINTING CO LTD
PI JP 07168532 A 19950704 Heisei
AI JP 1993-314899 (JP05314899 Heisei) 19931215
PRAI JP 1993-314899 19931215
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995
AB PURPOSE: To produce a display having the lessened unevenness of **image** display by using an array of electron releasing elements produced by providing the surfaces of emitter **wiring layers** with metallic films which are not etched by etching of insulating films and have an **electrical conductivity**.
CONSTITUTION: This electron releasing element has the emitter **wiring layers** 11 on an insulating substrate 10, the insulating layers 13 on the emitter **wiring layers** 11, gate electrode 14 layers, plural small **holes** of a required size formed on the insulating layers 13 and the gate electrode 14 layers and emitter electrodes 17 having pointed front ends within these small **holes**. The metallic connecting layers 12 which are not etched by etching of the insulating layers 13 and can make electrical connection between the emitter electrodes 17 and the emitter **wiring layers** 11 are formed between the emitter **wiring layers** 11 and the emitter electrodes 17 in the bottom parts of the small **holes**. As a result, the distances between the emitter electrodes 17 having the pointed front ends and the gate electrodes 14 are made uniform over the entire surface of the large-area substrate 10 and the electron releasing element having uniform and stable quality over the entire surface of the substrate 10 is obtd.
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L19 ANSWER 41 OF 41 JAPIO COPYRIGHT 2002 JPO
AN 1993-326611 JAPIO
TI SEMICONDUCTOR DEVICE
IN MURANAKA KIYOHIKO
PA NEC CORP
PI JP 05326611 A 19931210 Heisei
AI JP 1992-157460 (JP04157460 Heisei) 19920525
PRAI JP 1992-157460 19920525
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1993
AB PURPOSE: To block corrosion of upper **wiring layer** from spreading through a through **hole** part into a lower **wiring layer** by plugging the through **hole** part with a bonding wire and **electrically conducting** the upper and lower **wiring layers** through the bonding wire.
CONSTITUTION: Ball 1a of a bonding wire 1 is bonded through a through **hole** part 7 to a lower **wiring layer** 5. The through **hole** part 7 is plugged with the ball 1a of the bonding wire 1 while upper and lower **wiring layers** 3, 5 are **conducted electrically** through the bonding wire 1. Since

the **wiring layers** are isolated vertically and the through **hole** part for conducting the upper and lower **wiring layers** is plugged with the bonding wire, corrosion of upper **wiring layer** 3 is blocked from spreading to the lower **wiring layer** thus preventing deterioration of characteristics.

L28 ANSWER 1 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 1998-373118 [32] WPIX
DNN N1998-292763
TI Thermistor with high resistance value - has insulating layers which fuse and is absorbed in electrically conductive paste **coated** on **lead wires**, in case of glass sealing, to **electrically connect lead wires** and electrode **layers**.
DC V01
PA (MITV) MITSUBISHI MATERIALS CORP
CYC 1
PI JP 10149903 A 19980602 (199832)* 7p
JP 3275739 B 20020422 (200234) 7p
ADT JP 10149903 A JP 1996-304743 19961115; JP 3275739 B JP 1996-304743 19961115
FDT JP 3275739 B Previous Publ. JP 10149903
PRAI JP 1996-304743 19961115
AB JP 10149903 A UPAB: 19980812
The thermistor has electrode layers (1) individually formed on two opposing surfaces of a thermistor **chip** (2). **Lead wires** (4) **coated** with electrically conductive heat-resistant paste containing glass frit, are pinched at the edges of the thermistor **chip**. A glass tube is inserted to the junction of each **lead** wire. A glass sealing process is simultaneously performed with electrode layer baking to form a **circular lead** type glass coat thermistor.

After forming the electrode layers on the opposing surfaces of the thermistor **chip**, insulated inorganic-substance layers are formed on the surfaces on which the electrode layers are formed. In case of glass sealing process, the insulated layers react, fuse and absorbed in the electrically conductive paste and the **lead** wires are **electrically connected** to the electrode layers.

ADVANTAGE - Productivity and operability is improved since variation of resistance value is reduced. Resistance value is increased by reducing electrode layers. Prevents scaling of electrode layers since each electrode layer is insulated with inorganic substance layer.
Dwg.1/1

L28 ANSWER 2 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 1991-089273 [13] WPIX
DNN N1991-069007
TI Superconductor sensor for measuring temperature and magnetic field - has intermediate compressible insulating layer and outer malleable layer on high current carrying superconductors.
DC S01 S03 X12
IN HOLLANDER, M B; MCKINLEY, W E
PA (OMEG-N) OMEGA ENG INC
CYC 6
PI GB 2236192 A 19910327 (199113)*
DE 4027481 A 19910411 (199116)
CA 2023308 A 19910306 (199120)
FR 2651583 A 19910308 (199120)
US 5030614 A 19910709 (199130)
JP 04278469 A 19921005 (199246)# 8p
GB 2236192 B 19940323 (199409) 1p
DE 4027481 C2 19951102 (199548) 8p
CA 2023308 C 19960430 (199627)
ADT GB 2236192 A GB 1990-17241 19900807; DE 4027481 A DE 1990-4027481 19900830; US 5030614 A US 1989-402672 19890905; JP 04278469 A JP 1991-31188 19910227; GB 2236192 B GB 1990-17241 19900807; DE 4027481 C2 DE

1990-4027481 19900830; CA 2023308 C CA 1990-2023308 19900815
PRAI US 1989-402672 19890905
AB GB 2236192 A UPAB: 19930928
The sensing assembly comprises a relatively small and light-weight superconductive sensor conductor, whose primary purpose and design is not to carry high current loads, with little or no shunting ability, positioned in close proximity to a high current-carrying superconductor; and **electrical** current source **connected** to establish relatively low energy electrical current flow between the ends of the sensor conductor and, an indicating device for monitoring the flow of electrical current through the sensor conductor to detect changes therein which are indicative of changes in the critical parameters of the environment surrounding the assembly.

The sensor conductor structure has a core of superconductive material, a surrounding body of insulating material and an outer sheath of malleable material surrounding the insulating body, to provide structural strength and integrity.

ADVANTAGE - Prevents damage to superconductor.

L34 ANSWER 1 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1999-034210 [03] WPIX
DNN N1999-025554 DNC C1999-010316
TI High density multilayered printed wiring board, multi-**chip** carrier, and semiconductor package - with improved heat dissipation properties.
DC A85 L03 U11 U14 V04
IN INOUE, T; NODA, K; YUAN, B
PA (IBIG) IBIDEN CO LTD
CYC 1
PI US 5841190 A 19981124 (199903)* 44p
ADT US 5841190 A WO 1995-JP964 19950519, US 1996-601046 19960223
PRAI US 1996-601046 19960223
AB US 5841190 A UPAB: 19990122
High density multi-**layered** printed **wiring** board (pwb) (23) comprising; (16) Substrate with a higher heat conductivity than resins. (17) Build up layer on the first side of the substrate and having (I1 - 14) interlayer insulation and (C1 - C5) conductive layers that are alternately laminated formed on a first side (S1) , and with (19) an electronic parts mounting area and (21) first set of in / out terminals defined on its top surface. (13) Substrate supporter for mounting the pwb and defining a (24) window portion formed and dimensioned for supportive receipt of the pwb such that its opposite (S2) second surface is exposed from the window, the supporter including a second set of I / O terminals connected to the first. Also claimed is a multi-**chip** carrier assembly comprising the pwb above in which the first set of I / O are provided in an area between the parts mounting area and the edge of the substrate. A set of bonding pads surround the window with a second set of I / O surrounding them, and there is at least one **conductive** pattern for **electrically connecting** respective bonding pads and respective first I / O terminal. Also, a semiconductor package comprising the pwb and multi-**chip** carrier as above and including electronic parts (14,15) mounted on the parts mounting area, and a package as above in which the substrate supporter is a **lead** frame with **leads** surrounding an island supporting the pwb with the **leads electrically connected** to the first set of I / O of the build up layer.
USE - Semiconductor packaging including printed wiring boards and **chip** carriers.
ADVANTAGE - The package is cheap to make and has excellent heat dissipation properties.
Dwg.1,4/30

L34 ANSWER 2 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1998-588824 [50] WPIX
DNN N1998-459139
TI Thermal head substrate - connects **lead** pattern of heat generation element and **electrically conductive** layer either directly or via circuit **chip**.
DC P75 T04 U14
PA (GRAP-N) GRAPHTEC KK
CYC 1
PI JP 10264430 A 19981006 (199850)* 4p
ADT JP 10264430 A JP 1997-91721 19970325
PRAI JP 1997-91721 19970325
AB JP 10264430 A UPAB: 19981217
The substrate connects heat generation element (14) with an **electrically conductive** pattern (122) and forms a thermal head. A protective layer is provided so that a portion of **electrically conductive** layer is exposed. A circuit

chip is linked to each heat generation element.

The circuit **chip** is **connected** with the **electrically conductive** pattern such that a portion of the circuit **chip** overlaps on the protective **layer**. **Wire** bonding connection of the circuit **chip** and the exposed portion of the **electrically conductive** pattern is performed. When a circuit **chip** is not used, the **lead** pattern (141) of the heat generation element and the **electrically conductive** layer is performed, directly.

ADVANTAGE - Enables to connect heat generation element and **electrically conductive** pattern either directly or via circuit **chip**.

Dwg.1/4

L34 ANSWER 3 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1998-373118 [32] WPIX
DNN N1998-292763
TI Thermistor with high resistance value - has insulating layers which fuse and is absorbed in **electrically conductive** paste **coated** on **lead wires**, in case of glass sealing, to **electrically connect lead wires** and electrode **layers**.
DC V01
PA (MITV) MITSUBISHI MATERIALS CORP
CYC 1
PI JP 10149903 A 19980602 (199832)* 7p
JP 3275739 B 20020422 (200234) 7p
ADT JP 10149903 A JP 1996-304743 19961115; JP 3275739 B JP 1996-304743 19961115
FDT JP 3275739 B Previous Publ. JP 10149903
PRAI JP 1996-304743 19961115
AB JP 10149903 A UPAB: 19980812
The thermistor has electrode layers (1) individually formed on two opposing surfaces of a thermistor **chip** (2). **Lead wires** (4) **coated** with **electrically conductive** heat-resistant paste containing glass frit, are pinched at the edges of the thermistor **chip**. A glass tube is inserted to the junction of each **lead** wire. A glass sealing process is simultaneously performed with electrode layer baking to form a circular **lead** type glass coat thermistor.

After forming the electrode layers on the opposing surfaces of the thermistor **chip**, insulated inorganic-substance layers are formed on the surfaces on which the electrode layers are formed. In case of glass sealing process, the insulated layers react, fuse and absorbed in the **electrically conductive** paste and the **lead** wires are **electrically connected** to the electrode layers.

ADVANTAGE - Productivity and operability is improved since variation of resistance value is reduced. Resistance value is increased by reducing electrode layers. Prevents scaling of electrode layers since each electrode layer is insulated with inorganic substance layer.

Dwg.1/1

L34 ANSWER 4 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1998-151480 [14] WPIX
DNN N1998-120575
TI Semiconductor device e.g. for LSI - has set of metallic columnar members in resin substrate for providing **electrical connection** between its front and back sides.
DC U11
PA (TOSE-N) TOYO SEIMITSU KOGYO KK

CYC 1
PI JP 10022440 A 19980123 (199814)* 7p
ADT JP 10022440 A JP 1996-266528 19960829
PRAI JP 1996-146380 19960501
AB JP 10022440 A UPAB: 19980406
The semiconductor device consists of a set of **electrically conductive** metallic columnar members provided in a resin substrate (1). An LSI **chip** (6) with a wire bonding terminal is **electrically connected** to a **wiring layer** (3) of substrate on one side.
The metallic columnar members serve as an external terminal (4). **Electrical connection** between the resin substrate is carried out through the metallic columnar members.
ADVANTAGE - Improves reliability. Attains superior electrical property. Eases selection of size of insulating layer.
Dwg.1/9

L34 ANSWER 5 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1998-107487 [10] WPIX
DNN N1998-086468
TI Mounting method for flip-**chip** on **flexible wiring** board - involves temporarily fixing semiconductor bare **chip** and **flexible wiring** board using adhesive agent and then allowing to harden before **connecting electrically conductive** protrusion to **lead** pattern.
DC U11 V04
PA (OLYU) OLYMPUS OPTICAL CO LTD
CYC 1
PI JP 09331148 A 19971222 (199810)* 5p
ADT JP 09331148 A JP 1996-145860 19960607
PRAI JP 1996-145860 19960607
AB JP 09331148 A UPAB: 19980309
The method involves temporarily fixing a semiconductor bare **chip** (1) and a **flexible wiring** board (3) using an adhesive agent for temporal fix (6) between them.
When the adhesive agent for temporal fix hardens, the **electrically conductive** protrusion (2) of the semiconductor bare **chip** and the **lead** pattern (3a) of the **flexible wiring** board are **connected electrically**. The **flexible wiring** board and the semiconductor bare **chip** are sealed by injecting an insulating resin between them.
ADVANTAGE - Complicated holder is not needed since positional offset and stripping of junction of **flexible wiring** board and semiconductor bare **chip** due to handling after temporal fix are prevented. Simplifies injection of insulating resin in gap between semiconductor bare **chip** and **flexible wiring** board since gap is maintained by hardening of adhesive agent for temporal fix.
Dwg.1/7

L34 ANSWER 6 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1998-093445 [09] WPIX
DNN N1998-074677
TI Double sided **flexible wiring** board with semiconductor base **chip** mounting facility - has patterns formed on front and back part to which **electrically conductive** protrusion of base **chip** is **connected electrically**.
DC V04
PA (OLYU) OLYMPUS OPTICAL CO LTD

CYC 1
PI JP 09321390 A 19971212 (199809)* 5p
ADT JP 09321390 A JP 1996-138799 19960531
PRAI JP 1996-138799 19960531
AB JP 09321390 A UPAB: 19980302
The wiring board (3) has facility for flip **chip** mounting of a semiconductor base **chip** (1).
Patterns (3a,3e) are formed on front and back parts to which **electrically conductive** protrusion (2) of the **chip** is **connected electrically**.
ADVANTAGE - Enables to perform electric connection between surface **lead** pattern of wiring board and **electrically conductive** protrusion of **chip**, reliably.
Dwg.1/5

L34 ANSWER 7 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1996-347570 [35] WPIX
DNN N1996-292858
TI Bump mfg method for bonding LSI **chip** to **lead** frame - involves forming pad on **wafer** surface for every LSI **chip** on which bump is formed by electrolytic plating method.
DC U11
PA (KAWI) KAWASAKI STEEL CORP
CYC 1
PI JP 08162456 A 19960621 (199635)* 9p
ADT JP 08162456 A JP 1994-303763 19941207
PRAI JP 1994-303763 19941207
AB JP 08162456 A UPAB: 19960905
The method involves forming an interlayer insulating film on the surface of a **wafer** at both ends. Between the insulating film, a scribed line (12) is formed. A **wiring layer** which has a layer used as a **reflective** prevention film is formed on the surface of the insulating film. Then patterning of the **wiring layer** is carried out. A pad (18) is formed on the **wafer** for every LSI **chip** an a wiring (14) is formed between the scribed line and the pad. All the pads on the **wafer** are **connected electrically** and current is supplied to the pads through the wiring.
A passivation film is formed all over the **wafer** surface and then patterning of the film is carried out. Then a photoresist is formed on the surface of the **wafer** and patterning of the resist is carried out. Thus, the bump is formed on all the pads by electrolytic plating method and the photoresist is then removed.
ADVANTAGE - Eliminates formation and etching process of UBM. Reduces mfg time.
Dwg.1/9

L34 ANSWER 8 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1996-293266 [30] WPIX
DNN N1996-246541 DNC C1996-093506
TI Wiring board for semiconductor element - has **electrically conductive** member to connect divided parts of each set of metallise **wiring layer** electrically.
DC L03 U11 V04
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 08125064 A 19960517 (199630)* 5p
ADT JP 08125064 A JP 1994-265156 19941028
PRAI JP 1994-265156 19941028
AB JP 08125064 A UPAB: 19960731
The wiring board has a set of metallized **wiring layers**

(2) which are set on a substrate (1). A set of external **lead** terminals (3) are connected to each of the cell of the metallized **wiring layer** at one end.

The other end of the set of external **lead** terminals are connected to a frame like metal member (6). Each of the set of the metallize **wiring layers** is divided into two. The divided parts is then **connected electrically** to a **conductive** member (7).

ADVANTAGE - Enables switching of semiconductor element without deformation of external **lead** terminal. Enables to examined semiconductor element without isolating external **lead** terminal. Dwg.2/6

L34 ANSWER 9 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1996-274869 [28] WPIX
DNN N1996-231255
TI Quad-flat ceramic semiconductor device - has cap which airtight seals semiconductor **chip** to substrates where electrode is connected to **lead** terminal through wire.
DC U11
PA (FUIT) FUJITSU LTD; (SHIA) SHINKO DENKI KOGYO KK
CYC 1
PI JP 08115994 A 19960507 (199628)* 8p
ADT JP 08115994 A JP 1994-249430 19941014
PRAI JP 1994-249430 19941014
AB JP 08115994 A UPAB: 19960719
The device (11) has a substrate (17) where a first **wiring film** (13a) is set up. **Lead** terminals (12a,12b) are **electrically connected** to a semiconductor **chip** (18). An electrode (18a) provided for the semiconductor **chip** is connected to the terminal **lead** through a wire (14).

A cap (16) does the airtight sealing of the semiconductor **chip** to the substrate. An **electrically conductive** pin (20) connects the substrate and a wiring board (61), where a second **wiring film** (13b) is formed.

ADVANTAGE - Enables **wiring film** area to be extended. Enables signal current to be switched at high frequency when semiconductor **chip** is mounted. Provides bigger capacity for semiconductor device. Reduces wiring inductance. Simplifies package mfg. process. **Electrically connects** desired position between wiring boards. Increases package intensity and reliability. Dwg.1/8

L34 ANSWER 10 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1996-194149 [20] WPIX
CR 1996-177800 [18]
DNN N1996-162761 DNC C1996-061577
TI Semiconductor light emitting element - combines sub mount member and element main part with conducting state between P-side electrode and auxiliary P side electrode layer, reducing number of wire bonds on **lead** frame and providing high intensity characteristics.
DC L03 P81 U12
IN SHAKUDA, Y
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 08064872 A 19960308 (199620)* 7p
US 5557115 A 19960917 (199643) 12p
ADT JP 08064872 A JP 1994-194224 19940818; US 5557115 A US 1995-513624 19950810
PRAI JP 1994-194224 19940818; JP 1994-189565 19940811
AB JP 08064872 A UPAB: 19961104

The semiconductor light emitting element (1) forms a N-type semiconductor layer (4), a light emitting layer (5), and a P-type semiconductor layer (6) on the surface of a transparent insulating substrate (3). An element main part (2) forms N-side electrode (9) and a P-side electrode (10) to each exposure part of the semiconductor layers and the light emitting layer. A sub- mount member (11) has an auxiliary P-side electrode layer (14) and an auxiliary N-side electrode layer (15) on the surface of an **electrically conductive** state (12).

The surfaces of both the sub-mount member and the element main part are arranged opposite to each other. The sub mount member and the element main part are combined and the conducting state between the P side electrode and the auxiliary P side electrode layer becomes functional.

ADVANTAGE - Reduces number of wire bonds to **lead** frame. Simplifies wire connection work. Provides high intensity characteristic. Dwg.3/10

L34 ANSWER 11 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1996-126112 [13] WPIX
DNN N1996-106222
TI Optimum **integrated circuit** socket for semiconductor device inspection - has substrate for **connection** with **electrically conductive** layers arranged to correspond to electrodes of bare **chip** for inspection with wiring connected to conductive layers.
DC S01 U11
PA (YAWA) NIPPON STEEL CORP
CYC 1
PI JP 08022875 A 19960123 (199613)* 5p
ADT JP 08022875 A JP 1994-175972 19940705
PRAI JP 1994-175972 19940705
AB JP 08022875 A UPAB: 19960405
The socket (1) includes **electrically conductive** layers arranged in a substrate for connection (6) corresponding to the electrode parts of a semiconductor **chip** (7) which should be inspected. The substrate for connection is held by a substrate holder (5).

It has metal balls (10) whose arrangement junctions are made on each through hole (8) part of the substrate. Wiring (9) is connected to each metal ball, is provided which comes in contact to the contact (11a) of an external connector terminal (11).

USE/ADVANTAGE - For electric test of semiconductor device mounted in circuit substrate without using **lead** for external connection. Eliminates reformation of bump or excellent-article **chip** of solder after test. Enables remarkably simplified process inspection of manufacturing process. Inspects semiconductor **chip** easily and reliably even on bare **chip** which has bump in electrode part. Obtains very large applicability on various types of semiconductor **chips** without bumps in electrode parts. Dwg.1/8

L34 ANSWER 12 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1994-352720 [44] WPIX
CR 1994-345172 [43]; 1995-334272 [43]
DNN N1994-276957
TI Semiconductor device of surface mounting type ceramic package - by assigning predetermined function to divided metal film formed on substrate, and performs layer-to-layer **electrical connection**.
DC A85 L03 U11
IN HAMANO, T; HAYAKAWA, M; IKEMOTO, Y; KUBOTA, Y; MIYAJI, N; SAIGO, Y; SAKODA, H; SONO, M; TSUJI, K; YAMAGUCHI, I; YONEDA, Y
PA (FUIT) FUJITSU LTD; (FUIT) KYUSHU FUJITSU ELECTRONICS KK

CYC 3
PI JP 06275761 A 19940930 (199444)* 7p
US 5497032 A 19960305 (199615) 37p
US 5804468 A 19980908 (199843)
KR 119464 B1 19971027 (199948)
ADT JP 06275761 A JP 1993-57527 19930317; US 5497032 A US 1994-213720 19940316; US 5804468 A Div ex US 1994-213720 19940316, US 1995-561421 19951121; KR 119464 B1 KR 1994-5376 19940317
FDT US 5497032 A JP 06268091, JP 06275761; US 5804468 A Div ex US 5497032
PRAI JP 1993-57527 19930317; JP 1993-56252 19930317; JP 1994-20642 19940217
AB JP 06275761 A UPAB: 19991122
The semiconductor device (31) consists of a semiconductor **chip** (34) which is carried on the metal film (33) formed on a substrate (32). An electric connection is performed between the semiconductor **chip** and metal electric conductor (39), carried out by low melting glass (36) on the upper part of substrate. The electric conductor is arranged surrounding the semiconductor **chip** and metal film.
The semiconductor device is divided by the metal film into predetermined number and sealed by low melting glass (38, 43) and the lid part (44). The device provides **electrical connection** which is predetermined, to each divided metal film.
ADVANTAGE - Improves speed by improving electrical property. Reduces inductance, relative permittivity and resistance values.
Dwg.1/8

L34 ANSWER 13 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1994-184783 [23] WPIX
DNN N1994-145932 DNC C1994-083716
TI **Integrated circuit chip** composite - has **electrically conductive lead connected** to a conductive site on the **IC** by **wire** which is **coated** with dielectric material comprising Parylene.
DC A85 L03 U11
IN ZECHMAN, J H
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI EP 601323 A1 19940615 (199423)* EN 7p
R: DE FR GB
JP 06216183 A 19940805 (199436) 4p
US 5622898 A 19970422 (199722) 4p
US 5656830 A 19970812 (199738) 4p
US 5824568 A 19981020 (199849)
ADT EP 601323 A1 EP 1993-117486 19931028; JP 06216183 A JP 1993-308302 19931208; US 5622898 A Div ex US 1992-988849 19921210, US 1995-445381 19950519; US 5656830 A US 1992-988849 19921210; US 5824568 A Div ex US 1992-988849 19921210, Cont of US 1995-445381 19950519, US 1996-675822 19960705
FDT US 5824568 A Cont of US 5622898, Div ex US 5656830
PRAI US 1992-988849 19921210; US 1995-445381 19950519; US 1996-675822 19960705
AB EP 601323 A UPAB: 19940727
A composite comprises an **integrated circuit chip** carrying an **electrically conductive** site; an **electrically conductive lead**; and an **electrically conductive** wire interconnecting the conductive site and the **electrically conductive lead**. The **wire** is conformably **coated** with a dielectric material.
Pref. the **electrically conductive** site is Al and the **electrically conductive lead** is of Cu or

Au-plated Cu. The dielectric material is esp. Parylen (RTM) and esp. Parylene N having the formula -(-CH2-p-C6H4-Ch2-)- with a mol. wt. of ca. 500,000. The connecting wire is pref. of Au and is e.g. 0.0005-0.003 inches thick and at least about 5 mm long. The dielectric layer is deposited e.g. by vapour deposition and is e.g. 0.0001 to 0.001 inches, esp. 0.0001-0.0003 inches thick. Pref. the **chip**, the wire and a portion of the conductive **lead** are conformably coated with the dielectric material. The dielectric layer is overcoated with an **electrically conductive** coating e.g. of Al. The assembly is encapsulated by moulding e.g. in an epoxy encapsulating compsn..

USE/ADVANTAGE - Esp. in **integrated circuit** packages comprising an **integrated circuit** connected to conductive **leads** by connecting wires, whereby the asesmbly is encapsulated into a package by a moulding process.

The conformable dielectric coating on the connecting wires prevents short circuiting of the wires if they are distorted during the moulding process, and thus avoids the need for the relatively high tolerances involves with the use of relatively short connecting wires drawn very tightly between the **IC chip** and the connecting **leads** to avoid short circuiting, as has been used previously. Dwg.2/2

L34 ANSWER 14 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1992-020784 [03] WPIX
DNN N1996-347618 DNC C1996-130175
TI Bonding wire with heat and abrasion resistant coatings - comprising a fine wire with an inner coating of one non-conductive resin and another coating of a different non-conductive resin.
DC A28 A85 L03 U11 V04
IN KIMURA, M; KONDO, H; ONODERA, K; TATSUMI, K
PA (YAWA) NIPPON STEEL CORP; (NITE-N) NIPPON TEXAS INSTRUMENTS; (TEXI) TEXAS INSTR INC
CYC 2
PI JP 03270142 A 19911202 (199203)*
US 5554443 A 19960910 (199642)B 6p
ADT JP 03270142 A JP 1990-68423 19900320; US 5554443 A Cont of US 1991-672275 19910320, US 1995-440177 19950512
PRAI JP 1990-68423 19900320
AB US 5554443 A UPAB: 19961021 ABEQ treated as Basic

A bonding wire for use in forming bonded **electrical connections** on a semi-conductor device comprises: (a) an elongated fine wire of **electrically conductive** material; and (b) first and second non-conductive coating layers of different resins. The first non-conductive **coating** covers the **wire** and comprises at least one aromatic polyester resin having good insulating property and heat resistance. The second non-conductive resin layer covers the first non-conductive resin and comprises at least one resin selected from polyurethanes, polyester imides and polyimides having good abrasion resistance. Also claimed is a bonding wire as above, in which the wire is gold of dia. 30 micron and the coatings have a thickness of 0.1-1.2 and 0.1-1.0 micron resp. and a total thickness of 0.3-1.6 micron.

USE - For connecting **leads** to electrodes (pads) on a semiconductor **chip**.

ADVANTAGE - The double-**layer coated wire** has superior insulation properties, heat resistance and bonding property, and superior abrasion resistance to allow it to be clamped and handled during the connection process. The **chip** may be connected without requiring a special apparatus having fluid blowing and suction capabilities. Peeling flaws and short circuits between the wires or between a wire and the semiconductor **chip** are avoided. The **lead** distance may be reduced, allowing very large scale

integrated circuits to be constructed with high product yield and value.
Dwg.0/2

AB JP 03270142 A UPAB: 19961021
The device comprises a first crucible of insulation material contg. conductive vapour source, and a second crucible on the outside of the crucible with a first electrode of conductive material, and a second electrode of a high fusing point metal extending from the outside of the first and second crucibles to the inside of the first crucible, to measure an electric resistance between the vapour source and the second crucible.
USE - Cracks, etc., in the crucible can be detected at an earily stage. @(4pp Dwg.No.1/4)@

L34 ANSWER 15 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1990-300558 [40] WPIX
CR 1990-248449 [33]
DNN N1990-231032
TI **Image** sensor **chip** having multiple light receiving elements - has switch connected to one circuit line, and resets connected to other output line, simultaneously controlled NoAbstract Dwg 1/3.
DC S06 W02
IN NAKAMURA, K; OHZU, H; UENO, I
PA (CANO) CANON KK
CYC 6
PI JP 02210949 A 19900822 (199040)*
US 5262870 A 19931116 (199347) 11p
EP 382568 B1 19940615 (199423) EN 14p
R: DE FR GB NL
ADT JP 02210949 A JP 1989-30017 19890210; US 5262870 A Cont of US 1990-476769 19900208, US 1992-860587 19920330; EP 382568 B1 EP 1990-301416 19900209
PRAI JP 1989-30017 19890210; JP 1989-87892 19890410
AB JP 02210949 A UPAB: 19940803
Gate array mother **wafer** structure material comprises substrate numbers of base cells arrayed on substrate, and insulating film laminated on semiconductor elements of substrate. Required logical circuit is obtd. by wiring of base cells. Wiring part is arrayed at portion on insulating film corresponding to each semiconductor element, and second insulating film is uniformly laminated on plane where wiring part is arrayed. Connecting openings which **lead** to electrode and wiring part are formed at portion of insulating film corresponding to electrodes of each semiconductor element and at portion of second insulating **film** corresponding to **wiring** part. Conductive material is filled in each connecting opening.
USE/ADVANTAGE - Used for semiconductor devices. Quick turn around time (QTAT) and deg. of integration of material are improved. @(11pp Dwg.No.1,2/11)@

L34 ANSWER 16 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1990-126146 [17] WPIX
DNN N1990-097713 DNC C1990-055350
TI Overcurrent preventive diode - has two **leads** with one connected to diode **chip** surface by fuse **wire** through insulating **layer**.
DC A85 U11 U12
IN KOSUMI, Y; KURITA, Y; TAKAMI, K; TANAKA, K
PA (ROHL) ROHM CO LTD
CYC 6
PI EP 364981 A 19900425 (199017)*
R: DE FR GB NL
US 4945398 A 19900731 (199033)
EP 364981 B1 19931222 (199351) EN 8p

R: DE FR GB NL
DE 68911644 E 19940203 (199406)
KR 9303554 B1 19930506 (199421)
ADT EP 364981 A EP 1989-119341 19891018; US 4945398 A US 1989-421761 19891016; EP 364981 B1 EP 1989-119341 19891018; DE 68911644 E DE 1989-611644 19891018, EP 1989-119341 19891018; KR 9303554 B1 KR 1989-15081 19891020
FDT DE 68911644 E Based on EP 364981
PRAI JP 1988-137016U 19881020
AB EP 364981 A UPAB: 19930928
A diode comprises a **chip** (2) having two **leads** with ends secured to respective **chip** surfaces for **electrical** and heat **conduction**. One **lead** end (3a) is bonded to a surface (2a), and the other (4) is held against the surface with interposition of a thin electrical insulating layer (5) having an opening (5a) for exposing an **electrical connecting** part (6) of the surface.

The second **lead** end (4a) has an opening (4c) aligned with that in the layer and held in heat conduction with the **chip** via the layer. The second **lead** end is connected to the surface by a fuse (7) which is melt-cut on passage of a given over-current. The wire is pref. of Au, Ag, Cu, Al or Au-plated Ag. The layer is pref. of epoxy resin adhesive or glass, and the **chip** and **lead** ends are enclosed by a moulded body with inner part of silicone resin and outer part of epoxy resin.

USE/ADVANTAGE - Used e.g. is a rectifying diode for operation with a large current, eliminates the need fo a separate protector, provides effective heat dissipation and is of low cost.
1/2

L34 ANSWER 17 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1989-101646 [14] WPIX
DNN N1989-077543
TI Customisable circuitry using programmable interconnect - has **wire** segment **layers** forming programmable junctions, with segment terminal ends selectively joined by short lengths.
DC U11 U14
IN CAREY, D H; WHALEN, B H
PA (MICR-N) MICROELECTRONICS & COMPUTER TECHN; (MICR-N) MICROELTRN COMPUTER
CYC 10
PI EP 310357 A 19890405 (198914)* EN 19p
R: DE FR GB IT SE
AU 8822835 A 19890406 (198921)
JP 01165134 A 19890629 (198932)
US 5132878 A 19920721 (199232) 19p
US 5165166 A 19921124 (199250) 29p
CA 1310099 C 19921110 (199251)
EP 310357 B1 19940713 (199427) EN 24p
R: DE FR GB IT SE
DE 3850629 G 19940818 (199432)
US 5438166 A 19950801 (199536) 30p
ADT EP 310357 A EP 1988-308996 19880928; JP 01165134 A JP 1988-245871 19880929; US 5132878 A Cont of US 1987-102172 19870929, US 1989-344534 19890425; US 5165166 A Cont of US 1987-102172 19870929, Div ex US 1989-344534 19890425, US 1991-739344 19910909; CA 1310099 C CA 1988-578714 19880928; EP 310357 B1 EP 1988-308996 19880928; DE 3850629 G DE 1988-3850629 19880928, EP 1988-308996 19880928; US 5438166 A Cont of US 1987-102172 19870929, Cont of US 1989-344534 19890425, Cont of US 1991-739344 19910909, US 1992-979541 19921123
FDT US 5165166 A Div ex US 5107403; DE 3850629 G Based on EP 310357; US 5438166 A Cont of US 5132878, Cont of US 5165166
PRAI US 1987-102172 19870929; US 1989-344534 19890425; US 1991-739344

19910909; US 1992-979541 19921123

AB EP 310357 A UPAB: 19930923
The circuit comprises an interconnect for **connecting electrical** components, comprising a first set of essentially parallel wire segments. A second set of essentially parallel wire segments are non-planar and non-parallel to the first set of wire segments. Accessible programmable junctions are formed from the terminal ends of intersecting wire segments. The programmable junctions form diagonally extending programming tracks.

The wire segments are adaptable for selective linkage at the programmable junctions. A carrier film is bonded to the interconnect. An **integrated circuit chip** is bonded to the carrier film by **leads** extending from the carrier film to the interconnect. The bond site areas of adjacent **leads** are staggered with respect to one another along an axis joining the centre points of each of the bond sites.

ADVANTAGE - Interconnects of a variety of sizes can be formed.
2/18

L34 ANSWER 18 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1988-022735 [04] WPIX
DNN N1988-017266 DNC C1988-009996
TI Semiconductor device electrode structure and method - includes a silicide film, nitride film and electrode layer.
DC L03 U12
IN HORIUCHI, M; OWADA, N; TANEOKA, T; TSUNEOKA, M
PA (HITA) HITACHI LTD
CYC 5
PI EP 254035 A 19880127 (198804)* EN 9p
R: DE FR GB
JP 62298167 A 19871225 (198806)
US 5068710 A 19911126 (199150)
ADT EP 254035 A EP 1987-108781 19870619; JP 62298167 A JP 1986-140064 19860618; US 5068710 A US 1989-396687 19890822
PRAI JP 1986-140064 19860618
AB EP 254035 A UPAB: 20010910
Semiconductor device has an electrode structure comprising: semiconductor film, metal silicide film, conductive nitride film, and electrode or **wiring layer**. The latter is pref. an Al alloy. Silicide is pref. of Pt or Pd; nitride is pref. of Ti.

Semiconductor film is polySi opt. doped with B, As or P and of grain size smaller than the film thickness. The electrode is a bipolar transistor base **lead**-out, pref. connected to a p-base layer.

USE/ADVANTAGE - In e.g. a bipolar LSI or SICOS structure or a CMOSFET structure; device where electrode is an electrode of a bipolar transistor is claimed. Thermal degradation during wiring with Al is suppressed so that device reliability is enhanced. In an example contact is made to a polySi film base region through a via in an insulating layer by means of a 20nm Pd or Pt silicide film, a 100nm TiN film and an AlSi alloy base electrode layer. The contact resistance remains constant even after annealing for 10 hrs. at 475 deg. C.
Dwg.1/2

L34 ANSWER 19 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 2000-260813 JAPIO
TI SEMICONDUCTOR PACKAGING APPARATUS, TAPE THEREFOR AND METHOD OF PRODUCING THE APPARATUS
IN WATABE KAZUHIRO
PA TOSHIBA CORP
PI JP 2000260813 A 20000922 Heisei
AI JP 1999-58553 (JP11058553 Heisei) 19990305

PRAI JP 1999-58553 19990305
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To prevent short-circuit to adjacent patterns and eliminate limitation of a **chip** size due to increase of the number of bonding pads, by punching only the portion corresponding to a bonding pad of a **electrically conductive wiring layer** formed on a polymer film layer **electrically connecting** a **lead** to a semiconductor **chip**.
SOLUTION: In the portion 120 corresponding to a bonding pad of a semiconductor **chip** in a polymer film layer 110, the polymer film is punched, and a **lead** in a package is connected to the portion 120 by means of a wiring pattern 130. In this way, since an inner **lead** can enter the center of the **chip** and the wiring pattern 130 is fixed to the insulating polymer film layer 110, short-circuit of the wiring pattern 130 to the lower semiconductor **chip**, or short-circuit of the wiring pattern 130 to each other is prevented. Since the bonding pad can be provided on not only the perimeter of the **chip** but also the center of the **chip**, reduction of the **chip** size is not restricted even if the number of pads is increased.

L34 ANSWER 20 OF 26 JAPIO
AN 2000-188370 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN ICHIHARA SEIICHI; KIMOTO RYOSUKE; YAMADA MASARU; ISHIGAKI KIMIHISA; KAWAKUBO HIROSHI; AUCHI MAKOTO; KANEDA TAKESHI
PA HITACHI LTD
HITACHI ULSI SYSTEMS CO LTD
PI JP 2000188370 A 20000704 Heisei
AI JP 1998-365526 (JP10365526 Heisei) 19981222
PRAI JP 1998-365526 19981222
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide high density mounting of **chip** -laminated-type and small- sized semiconductor devices.
SOLUTION: This semiconductor device comprises a first thin-**film wiring** tape 3 supporting a first semiconductor **chip** 1 and provided with a first solder land 3a **electrically connected** to a first pad 1a of the first semiconductor **chip** 1, a second thin-**film wiring** tape 4 supporting a second semiconductor **chip** 2 and provided with a second solder land 4a **electrically connected** to a second pad 2a of the second semiconductor **chip** 2, a bump electrode 5 **electrically connecting** the first solder land 3a to the second solder land 4a, and an outer **lead** 4c which is projected from the second thin **film wiring** tape 4 as an external terminal and is bent towards the mounting substrate, and the first solder land 3a and the first pad 1a of the first semiconductor **chip** 1 **electrically connected** thereto, and the corresponding second solder land 4a and second pad 2a of the second semiconductor **chip** 2 **electrically connected** thereto are arranged at mirror **image** symmetrical positions.

L34 ANSWER 21 OF 26 JAPIO
AN 1999-198365 JAPIO
TI INK JET HEAD
IN FUJII MITSUYOSHI; MATSUMOTO SHUZO; MURAI TAEKO; NARUSE OSAMU
PA RICOH CO LTD
PI JP 11198365 A 19990727 Heisei

AI JP 1998-8106 (JP10008106 Heisei) 19980119
PRAI JP 1998-8106 19980119
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To realize a high density by a method wherein actuator elements and a driving circuit are connected together through a **flexible wiring** board and, at the same time, the driving circuit is mounted on the flexible board.
SOLUTION: In an electrical component unit 4, driving **ICs** 32 are mounted on a **flexible wiring** board 31 by providing the driving **ICs** 32, each of which is a driving circuit for applying driving wave forms to the piezoelectric elements of an actuator unit, trimming resistances 33 for adjusting the scatterings of ink drop speeds of respective nozzles, connecting terminals 34 to the actuator unit, connecting terminals 35 to a device main body and **lead** wire patterns 37 for **electrically connecting** the driving **ICs** 32 to the connecting terminal 35 to the device main body on the **flexible wire** board 31. Thus, even when the number of actuator elements increases as the **image** quality and the arrangemental density of parts become higher, the electrical wiring between the driving circuit and the actuator elements can be easily executed.

L34 ANSWER 22 OF 26 JAPIO
AN 1999-185004 JAPIO
TI **IC** MODULE AND **IC** CARD LOADING THE MODULE
IN ARAI KAZUE; YAMAGUCHI MIKIRO; MATSUMURA SHUICHI
PA TOPPAN PRINTING CO LTD
PI JP 11185004 A 19990709 Heisei
AI JP 1997-357030 (JP09357030 Heisei) 19971225
PRAI JP 1997-357030 19971225
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide an **IC** module capable of absorbing stress to bending and preventing the release of a resin mold part by folding the connecting piece of a **lead** frame along with the outside of the resin mold part, exposing the connecting piece on the resin mold part and **electrically connecting** it with a terminal for external connection.
SOLUTION: The **IC** module is provided with a **wiring** pattern **layer** 7 forming a terminal 2 for external connection, to which gold plating is performed, from copper or the like on one side of a substrate 8 composed of glass epoxy resin or the like by patterning copper or the like on the other side. The connecting piece of a **lead** frame 11 folded outside a resin mold part 4 and exposed on the resin mold part 4 is connected with the **wiring** pattern **layer** 7 by a solder bump 12. Further, the **wiring** pattern **layer** 7 and the terminal 2 for external **connection** are **electrically connected** by **conductive** plating performed to a through hole 3 through the substrate 8.

L34 ANSWER 23 OF 26 JAPIO
AN 1997-321390 JAPIO
TI DOUBLE-SIDED **FLEXIBLE WIRING** BOARD
IN TAKASUGI HIROSHI
PA OLYMPUS OPTICAL CO LTD
PI JP 09321390 A 19971212 Heisei
AI JP 1996-138799 (JP08138799 Heisei) 19960531
PRAI JP 1996-138799 19960531
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To ensure reliable **electrical**

connection between a **lead** pattern on the surface of a double-sided **flexible wiring** board and a conductive protrusion of a semiconductor bare **chip** by forming the pattern on the opposite sides of the double-sided **flexible wiring** board at a part where the conductive protrusion of the semiconductor bare **chip** is **connected electrically**.
SOLUTION: A rear pattern 3e is formed without fail at a part of a double-sided **flexible wiring** 3, to be **connected electrically** with the **conductive** protrusions 2 of a semiconductor bare **chip** 1, immediately below a plurality of surface **lead** patterns 3a. Consequently, planarity of the surface **lead** pattern 3a is kept when the semiconductor bare **chip** 1 is mounted on the double-sided **flexible wiring** 3, and the conductive protrusions 2 of a semiconductor bare **chip** 1 touch the surface **lead** pattern 3a on the double-sided **flexible wiring** 3 perfectly at a plurality of contacts. Perfect contact is ensured similarly for a case employing a conductive adhesive, a conductive sheet or diffusion of metals.

L34 ANSWER 24 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1993-218145 JAPIO
TI MULTILAYER **WIRING** TYPE **FILM** CARRIER
IN YAMAGUCHI KENJI; NAKADA YOSHIHIRO; TANAKA HIROKI; ONDA MAMORU; TAKAGI MASAHARU; MURAKAMI TOMIO
PA HITACHI CABLE LTD
PI JP 05218145 A 19930827 Heisei
AI JP 1992-22505 (JP04022505 Heisei) 19920207
PRAI JP 1992-22505 19920207
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1993
AB PURPOSE: To provide a new multilayer **wiring** type **film** carrier by which a bump of a **chip** to be mounted can be reliably connected to an inner and the connection can be inspected.
CONSTITUTION: This multilayer **wiring** type **film** carrier has at least a multilayer TAB film carrier 3 having a conductor layer to become an outer **lead** 6a and a multilayer TAB film carrier 3 having a conductor layer to become an inner **lead** 6b while **electrically connecting** the **conductor** layer to become the outer **lead** 6a to the conductor layer to become the inner **lead** 6b and having a plurality of kinds of extension length in the direction of the **chip** mounting part.

L34 ANSWER 25 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1984-215875 JAPIO
TI THERMAL PRINTING HEAD
IN KINOSHITA TADAYOSHI; NAMIKI KOJI
PA TOSHIBA CORP
PI JP 59215875 A 19841205 Showa
AI JP 1983-90627 (JP58090627 Showa) 19830525
PRAI JP 1983-90627 19830525
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AB PURPOSE: To perfectly connect a wiring circuit and conductors to each other and enable to enhance reliability of a head, by a method wherein opening parts are provided in an insulator **layer** made on **wiring** circuits, and **conductors** for **electrically connecting** the wiring circuits through the opening parts are provided.
CONSTITUTION: Heating resistors 112 are provided in a row on an insulated substrate 110 provided with a glaze layer 111, then the first and second

common electrode groups 114, 115 constituting the wiring circuits are connected thereto, and the first and second **IC** groups 116a ..., 117a ... are connected thereto. A common **lead** 11401 for the common electrode 114 is connected to a conductor wire 126 by an ultrasonic bonder through the opening part 113a provided in the insulator layer, while a common **lead** 11501 for the common electrode 115 is connected to a conductor wire 126 by an ultrasonic bonder through the opening part 113b. Accordingly, bond between the wiring circuits and the conductors is prevented from being broken by forces generated due to differences in therman expansion between the insulated substrate and the conductors or external forces, and reliability is enhanced.

L34 ANSWER 26 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1982-157581 JAPIO
TI PHOTOELECTRIC CONVERTER
IN UEDA TOMOSHI; TAKIGAWA HIROSHI; YOSHIKAWA MITSUO; ITO MICHIHARU; HAMASHIMA SHIGEKI
PA FUJITSU LTD
PI JP 57157581 A 19820929 Showa
AI JP 1981-43650 (JP56043650 Showa) 19810324
PRAI JP 1981-43650 19810324
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1982
AB PURPOSE: To simplify the connection of a photoelectric converter and to reduce the size of the converter by connecting the converter with a conductor layer without using a **lead** wire necessary for bonding when connecting a signal output from respective photodetecting elements to a trunk terminals.
CONSTITUTION: A **reflection** preventive film 24 is formed on a semiconductor substrate 22, a photodetector 23 is drawn with a thick insulating layer 25, and a plurality of photodetecting elements 26a∼26e thus formed are aligned in an array. Then, output **wire layers** 27a∼27e made of Au-deposited films **electrically connected** to the respective elements are connected through insulating films 25 to respective trunk terminals 34a∼34e. This connection is performed by forming a deposited layer of In using a metal mask of trunk conductive layers 33a∼33e having connecting pads 34a∼34e between the **wire layers** and the trunk terminal and connecting them each other. In this manner, the elements 26a∼26e and the terminals 34a∼34e can be contacted closely without gap, thereby reducing the size of a **chip**.

L35 ANSWER 1 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2001-205803 [21] WPIX
DNN N2001-147094 DNC C2001-061856
TI **Solid state** image pickup element module for micro camera, includes polyamide resin film which is bent and shaped orthopedically, so that **chips** are packaged.
DC A85 P31 S05 U13 W04
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 2001016486 A 20010119 (200121)* 5p
ADT JP 2001016486 A JP 1999-180774 19990625
PRAI JP 1999-180774 19990625
AB JP2001016486 A UPAB: 20010418
NOVELTY - A CCD **chip** (4) is mounted in **wiring layer** formation surface side of polyamide resin film (1). Semiconductor **chip** (5) and passive component (6) are mounted on the same **wiring layer** formation surface side of resin film. The resin film is bent and is orthopedically and cylindrically shaped, so that the **chips** (4,5) and component (6) are packaged.
DETAILED DESCRIPTION - A **wiring layer** (3) is formed on main surface of the resin film (1), which includes protruding inner **lead**. The electrode terminal of the CCD **chip** (4) and inner **lead** are connected. An optical glass (9) is bonded to another surface of the resin film. A cable (11) is connected to the edge of the **wiring layer**.
USE - For micro camera for endoscopes.
ADVANTAGE - Enables obtaining **solid state** image pickup element module of high resolution, with simplified manufacturing process.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of **solid state** image pickup element module.
Resin film 1
Chips 4,5
Passive component 6
Optical glass 9
Cable 11
Dwg.1/6

L35 ANSWER 2 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1998-147668 [14] WPIX
DNN N1998-116999 DNC C1998-048250
TI Fabrication of **solid state** imaging apparatus - with the device **chip** and relevant peripheral circuit **chips** mounted in the same planar package..
DC L03 U11 U13 U14 W04
IN ASAUMI, M; CHATANI, Y; SANO, Y; TANAKA, H; TERAKAWA, S
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 26
PI EP 828298 A2 19980311 (199814)* EN 16p
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC NL PT RO SE SI
JP 10084509 A 19980331 (199823) 10p
KR 98024076 A 19980706 (199926)
CN 1176556 A 19980318 (200209)
ADT EP 828298 A2 EP 1997-110313 19970624; JP 10084509 A JP 1996-236303 19960906; KR 98024076 A KR 1997-30492 19970701; CN 1176556 A CN 1997-115429 19970723
PRAI JP 1996-236303 19960906
AB EP 828298 A UPAB: 19980406
Imaging apparatus comprising; substrate on which a **solid**

state imaging device **chip** and peripheral circuit element **chips** are mounted, container with a recessed portion in which the substrate is placed, transparent cover body which seals the container to make a space inside the container. Also claimed is the apparatus in which the substrate is a semiconductor with wiring in its surface, and the cover is transparent in at least the imaging area of the **solid state** imaging device **chip**. Also claimed is the apparatus in which the cover body is opaque with a transparent window. Also claimed is a process form making the apparatus by; a) Forming in sequence a first insulating film, first thin **film** conductor **wiring**, second insulating **film**, second thin **film** conductor **wiring** on an electroconductive substrate. b) Mounting the imaging device and peripheral circuit **chips** on the substrate, connecting the electrode of each **chip** to either the first or second conductor wiring, and connecting the wiring to the external **lead** of the container. c) Hermetically sealing up the container with a cover body having a transparent portion corresponding to at least the imaging area of the **solid state** imaging device **chip**.

USE - **Solid state** imaging devices.

ADVANTAGE - Packaging of the device and circuit **chips** together suppresses deterioration of image quality and increases circuit density.

Dwg.1A/11

L35 ANSWER 3 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1997-124586 [12] WPIX
DNN N1997-102836
TI **Chip** type **solid state** electrolytic capacitor - in which cathode conductor layer and anode **lead** wire of capacitor element are pulled out of front face of case.
DC V01
PA (NIDE) NEC CORP
CYC 1
PI JP 09007891 A 19970110 (199712)* 6p
ADT JP 09007891 A JP 1995-155813 19950622
PRAI JP 1995-155813 19950622
AB JP 09007891 A UPAB: 19970320

The capacitor has a box type case (5) which accommodates a capacitor element (1). An anode **lead** wire (2) is linearly drawn out from the capacitor element. The capacitor element is sealed by filling the case with the insulating resin (7). A cathode conductor layer (8) is formed in outer front face of the capacitor element. A pair of electrically conductive layers (3,4) are formed on the front faces of the case.

The cathode conductor layer and the anode **lead** wire are connected to the conductive layers at the case through the respective conductive adhesives (6). The cathode conductor layer and the anode **lead** wire are pulled out of the front face of the case.

ADVANTAGE - Simplifies fixation and connection work. Prevents deformation of case caused by difference in coefficient of thermal expansion. Obtains good shape stability. Offers high density installation nature.

Dwg.1/4

L35 ANSWER 4 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1993-155526 [19] WPIX
DNN N1993-119189 DNC C1993-069296
TI **Chip**-shaped **solid state** electrolytic capacitor - forms anode metal layer on anode **lead** wire exposing from anode outgoing side of armour resin, and eliminates space for external terminal NoAbstract.
DC A85 L03 V01

PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 05090095 A 19930409 (199319)* 5p
ADT JP 05090095 A JP 1991-251081 19910930
PRAI JP 1991-251081 19910930

L35 ANSWER 5 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1982-D5066E [13] WPIX
TI **Chip solid state** capacitor manufacture - by using metal thin film to which **lead** wires are welded to improve shape and dimension.
DC V01
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 57030318 A 19820218 (198213)* 6p
PRAI JP 1980-104687 19800730

L35 ANSWER 6 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 2001-309244 JAPIO
TI **SOLID-STATE** IMAGING APPARATUS AND MOUNTING METHOD OF THE SAME
IN KONNO YOSHIHIKO
PA CANON INC
PI JP 2001309244 A 20011102 Heisei
AI JP 2000-117768 (JP2000117768 Heisei) 20000419
PRAI JP 2000-117768 20000419
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To solve the problems of the conventional technology such that at fixing an unit of a **solid-state** imaging device of CCD and CMOS or the like to an electronic camera by using TAB package technique, an extremely high accuracy of component machining is required, and that it is impossible to heat from the side of the camera for melting solder at the deep depth.
SOLUTION: In the **solid state** imaging apparatus comprising a **chip** 20 of slid state imaging device, the **chip** 20 has a land part 4 for electric wiring at the same surface side of a light receiving surface 3, a TAB tape 5 composed by a **flexible** printed **wiring** board having a **lead** part 7a connected to the land part 4 of the **chip** 20 and a cover glass 11 arranged opposite to the **chip** 20 getting caught in the tape 5, a metal film 13 is composed at the out of the light receiving area of the cover glass 11.
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L35 ANSWER 7 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 2001-298172 JAPIO
TI **SOLID-STATE** IMAGE PICKUP DEVICE
IN KITANI MITSUJI
PA CANON INC
PI JP 2001298172 A 20011026 Heisei
AI JP 2000-113810 (JP2000113810 Heisei) 20000414
PRAI JP 2000-113810 20000414
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a **solid-state** image pickup device for removing static electricity and preventing the destruction or deterioration of elements, by providing a transparent conductive film on the glass of a cap, conducting this **film** to the **wiring** of a **flexible** substrate and performing discharging through this film concerning a thin **solid-state** image pickup device, in a structure for sticking and sealing the glass of the gap on a **solid-state** imaging device

mounted on a TAB tape or the like.
SOLUTION: The configuration of the **solid-state** image pickup device with which a beam **lead** provided on a **flexible wiring** board is connected to a metal projection provided on the connecting part of the **solid-state** imaging device around an image pickup area of the **solid-state** imaging device **chip**, while making an opening part formed on the **flexible wiring** board correspondent to the image pickup area. The cap composed of transparent glass for protecting the **solid-state** imaging device **chip** is mounted so as to cover the opening part, the transparent glass and a seal layer are deposited in this order around the outer periphery of the **solid-state** imaging device **chip**, and the valid pixel area of the **solid-state** imaging device **chip** is surrounded with the seal layer. A transparent conductive film is provided on the cap while facing the valid pixel area.
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L35 ANSWER 8 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1999-354766 JAPIO
TI **SOLID STATE** IMAGE SENSOR
IN NAGAYOSHI RYOICHI; ITAKURA KEIJIRO
PA MATSUSHITA ELECTRON CORP
PI JP 11354766 A 19991224 Heisei
AI JP 1998-161847 (JP10161847 Heisei) 19980610
PRAI JP 1998-161847 19980610
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a micro **solid state** image sensor in which decrease in the ratio of light receiving area to the external area sue to reduction in size of the **solid state** image sensor is suppressed and the effect of on-**chip** microlens is not reduced.
SOLUTION: A **chip** 2 provided with a **solid state** image sensor and bonding pads 1 and a **flexible wiring** board provided with inner **leads** 9 are connected through bumps 10 at the end part of the bonding pads 1 and the inner **leads** 9. The inner **lead** 9 is bent at right angle along the side wall of the **chip** 2 and fixed thereto through a fixing agent 11. The **chip** 2 mounting a convex microlens 12 and a cover glass 3 are bonded through an adhesive 4 having refractive index lower than that of the microlens 12.
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L35 ANSWER 9 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1999-055574 JAPIO
TI IMAGE PICKUP DEVICE
IN ASAUMI MASASHI; TERAKAWA SUMIO; SANO YOSHIKAZU; CHATANI YOSHIKAZU
PA MATSUSHITA ELECTRON CORP
PI JP 11055574 A 19990226 Heisei
AI JP 1997-204982 (JP09204982 Heisei) 19970730
PRAI JP 1997-204982 19970730
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To obtain an image pickup device which performs multilayer wiring, is also miniaturized, also has a stable operation and a high S/N and does not have so much unnecessary radiation by using a semiconductor substrate instead of a glass epoxy substrate.
SOLUTION: Wiring 15 and 16 which are constituted of a metallic layer are formed and also a **solid-state** image pickup device **chip** 12 and a drive device **chip** 13 are mounted on a semiconductor substrate 11. A pad 14 is connected to the **chips** 12 and 13 through a metallic wire. The wiring 15 and 16 performs wiring

between pads of the **chips** 12 and 13 and to a pad 17, and the wiring 15 is formed by a 1st metallic **layer** and the **wiring** 16 is formed by a 2nd metallic layer. The pad is connected by a package **lead** terminal and a metallic wire. Then, the width of the wiring 15 and 16 can be made as thin as about 1 μm, a wiring area is made small, and therefore, it is possible to miniaturize an image pickup device. Also, a coupling capacity becomes small due to the reduction of the wiring area, and a stable operation of the image pickup device and a high SIN are accomplished.
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L35 ANSWER 10 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1988-318158 JAPIO
TI **SOLID-STATE** IMAGE SENSING DEVICE
IN IGUCHI TSUDOI; ABE HIDEAKI; KADOWAKI MASAHIKO; IZUMI AKIYA
PA HITACHI LTD
HITACHI DEVICE ENG CO LTD
PI JP 63318158 A 19881227 Showa
AI JP 1987-153328 (JP62153328 Showa) 19870622
PRAI JP 1987-153328 19870622
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To improve the quality of an image to be formed by a method wherein the outside surface of the optical effective surface of a transparent sealing cap is constituted lower than the other outside surface other than the optical effective surface of the cap.
CONSTITUTION: A **solid-state** image sensing device is constituted by sealing a **solid-state** image sensing element **chip** 2 mounted on a mounting substrate 1 with a transparent sealing cap 3. The substrate 1 is constituted of a substrate 1A, internal electrodes 1B and 1C, a **lead**-out wiring 1D, a connecting hole 1E, a connecting hole **wiring** 1F, a **coating** material 1G and an external electrode 1H. The outside surface of the optical effective surface A of the cap 3 is constituted lower compared to the other outside surface B other than the optical effective surface A of the cap 3 to make positively the contact of the cap with some things on the other outside surface B so as not generate damage of a flaw and so on. Moreover, a package member is constituted of the substrate 1 and the cap 3 having a cavity 3A.
COPYRIGHT: (C)1988,JPO&Japio

L35 ANSWER 11 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1988-147133 JAPIO
TI ENDOSCOPE
IN FUKUOKA YOSHITAKA
PA TOSHIBA CORP
PI JP 63147133 A 19880620 Showa
AI JP 1986-295408 (JP61295408 Showa) 19861210
PRAI JP 1986-295408 19861210
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To improve the resolution of an endoscope, to prolong its life, and to **lead** out image information as a television signal by sealing a **solid-state** image pickup element which constitute an image pickup means airtightly with a metallic cap having a transparent window.
CONSTITUTION: The **solid-state** image pickup element 8 is mounted on a **chip** carrier 7 and the metallic cap 9 with the glass window is arranged which seals the **solid-state** image pickup element 8 air-tightly. Further, a metallic frame 10 is arranged along the outer periphery of the metallic cap 9 with the glass window. This image pickup means 6 is fixed on a **flexible** **wiring** board 12 where circuit elements 11 such as a transistor,

plural resistance **chips**, and plural decoupling capacitors which form an emitter follower circuit for the impedance conversion of the image pickup signal from the **solid-state** image pickup element 8 are mounted. Then the joint part between the **chip** carrier 7 and **flexible wiring** board 12 is sealed with organic insulating resin 13. Consequently, the resolution is high, the life is long, and the image information can be led out as the television signal.

L36 ANSWER 1 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 2002-580488 [62] WPIX
DNN N2002-460790
TI **Chip** size package for mounting CCD, CMOS, includes side electrode on side insulating layer, which is electrically connected to connection wiring at backside insulating layer through rewiring layer.
DC U11 U13 W04
PA (CANO) CANON KK
CYC 1
PI JP 2002198463 A 20020712 (200262)* 7p
ADT JP 2002198463 A JP 2000-395625 20001226
PRAI JP 2000-395625 20001226
AB JP2002198463 A UPAB: 20020926
NOVELTY - A side electrode (2b) on a side insulating layer (3a), is electrically connected to a connection wiring at backside insulating layer (3b) through a rewiring layer (2a).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included **chip** size package manufacturing method.
USE - For mounting CCD, CMOS, optoelectric transducer, light receiving element, **solid-state image** pickup element, etc.
ADVANTAGE - The inexpensive package enables micromounting.
DESCRIPTION OF DRAWING(S) - The figure shows an external view of the **chip** size package. (Drawing includes non-English language text).
Rewiring layer 2a
Side electrode 2b
Side insulating layer 3a
Backside insulating layer 3b
Dwg.1/21

L36 ANSWER 2 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 2002-408942 [44] WPIX
DNN N2002-321314
TI **Solid state image** pick up element e.g. CCD camera has microlens and wiring whose surfaces are spin coated with resin.
DC P81 U11 U13
PA (SONY) SONY CORP
CYC 1
PI JP 2002009266 A 20020111 (200244)* 5p <--
ADT JP 2002009266 A JP 2000-188798 20000623
PRAI JP 2000-188798 20000623
AB JP2002009266 A UPAB: 20020711
NOVELTY - The rough surface of the microlens (12) and the **wiring** is **coated** with polymethyl methacrylate resin by spin coating. The resin coated film (13) is then polished.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **solid state image** element manufacturing method.
USE - **Solid state image** pick up element e.g. CCD camera.
ADVANTAGE - Eliminates adherence of dust on microlens surface, even when there may be dust adhering to **chip** surface. The dust adhered to the microlens surface is removed by blowing air, without damaging the **chip** and the wiring. Refractive index of overcoating layer is small and close to air, thereby the function of the **solid state image** pick up element is ensured.
DESCRIPTION OF DRAWING(S) - The figure shows an explanatory drawing of the process of cleaning the microlens surface. (Drawing includes non-English language text).
Microlens 12

Resin coated film 13
Dwg.4/9

L36 ANSWER 3 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 2002-320797 [36] WPIX
DNN N2002-251327
TI **Solid-state image** pick-up has groove formed in electric charge transfer electrode, in which insulating **film** and shunt **wiring** are formed.
DC U11 U13 W04
PA (SONY) SONY CORP
CYC 1
PI JP 2001352050 A 20011221 (200236)* 7p
ADT JP 2001352050 A JP 2000-169871 20000607
PRAI JP 2000-169871 20000607
AB JP2001352050 A UPAB: 20020610
NOVELTY - A groove (23) formed in the electric charge transfer electrode (22) is covered by an insulating film (24) over which an shunt wiring (25) is provided.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **solid-state image** pick-up manufacturing method.
USE - **Solid-state image** pick-up.
ADVANTAGE - The height of the on-**chip** lens is increased due to the thickness of the shunt wiring by which an exact focus on the receiver is obtained, with reduced smear and improved sensitivity.
DESCRIPTION OF DRAWING(S) - The figure explains the manufacturing process of **solid-state image** pick-up.
(Drawing includes non-English language text).
Electric charge transfer electrode 22
Groove 23
Insulating film 24
Shunt wiring 25
Dwg.1/6

L36 ANSWER 4 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 2001-262904 [27] WPIX
DNN N2001-188258
TI **Solid-state image** pickup element has shading film formed over shunt wiring whose height is greater than or equal to its width.
DC U13 W04
PA (SONY) SONY CORP
CYC 1
PI JP 2001053258 A 20010223 (200127)* 6p <--
ADT JP 2001053258 A JP 1999-221982 19990805
PRAI JP 1999-221982 19990805
AB JP2001053258 A UPAB: 20010518
NOVELTY - The **solid-state image** pickup unit (20) has shading film (10) formed over shunt wiring (21) whose height is greater than or equal to its width (h at least w). A portion (10c) of shading film is formed so that it does not cross-over the line connecting the aperture end (10b) and edge (12a) of on-**chip** lens (12). The straight line mentioned passes through vent (10a) formed on light sensor (3).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **solid-state image** pickup element manufacturing method.
USE - CCD **solid-state image** pickup element.
ADVANTAGE - By forming shunt wiring (h at least w), low resistance of

shunt wiring is obtained along with high speed operation of **solid -state** pickup element. Decrease in sensitivity due to lower condensing efficiency is prevented by forming shunt wiring (h at least w) so that condensing efficiency of lens is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of **solid-state image** pickup element. (Drawing includes non-English language text).

Light sensor 3
Shading film 10
Vent 10a
Aperture end 10b
Portion of shading film 10c
On-**chip** lens 12
Edge 12a
Solid-state image pickup unit 20
Shunt wiring 21
Dwg.1/4

L36 ANSWER 5 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 2000-519262 [47] WPIX
DNN N2000-384382
TI **Solid state image** pick up for electronic endoscope, has signal cable which is connected to terminal portion formed on edge of circuit board in **image** pick up **chip** projected area.
DC P31 P81 W04
PA (SONY) SONY CORP
CYC 1
PI JP 2000199863 A 20000718 (200047)* 6p
ADT JP 2000199863 A JP 1999-2094 19990107
PRAI JP 1999-2094 19990107
AB JP2000199863 A UPAB: 20000925
NOVELTY - Bonding pads (25) are formed at periphery of **solid state image** pick-up **chip** (18). Several other bonding pads provided to circuit board (20b) are electrically connected by connector (29) to have **film** that forms **wiring** pattern. Electronic component (19) is mounted in step surface of board. Signal cable (30) is connected to terminal portion (27) formed on edge of board, in **image** pick up **chip** projected area.

USE - For electronic endoscope, charge coupled device (CCD).

ADVANTAGE - Enables size reduction of **image** pick up unit. Narrow diameter of endoscope leading end is attained.

DESCRIPTION OF DRAWING(S) - The figure shows perspective diagram of fixed **image** pick up apparatus.

Image pick up **chip** 18
Electronic component 19
Circuit board 20b
Bonding pad 25
Terminal portion 27
Connector 29
Cable 30
Dwg.3/8

L36 ANSWER 6 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 2000-122421 [11] WPIX
DNN N2000-093410
TI **Solid-state image** pick-up for camera.
DC U11 U13 W04
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 1
PI JP 11354766 A 19991224 (200011)* 5p <--

ADT JP 11354766 A JP 1998-161847 19980610
PRAI JP 1998-161847 19980610
AB JP 11354766 A UPAB: 20000301
NOVELTY - The **solid-state image** pick-up has a **solid-state image** pick-up element formed on a **chip** (2). A micro lens (12) is configured on the **solid-state image** pick-up element. An adhesive agent (4) bonds a cover glass (3) on the micro lens and **chip**. The refractive index of the adhesive agent is different from the refractive index of the micro lens.
USE - For camera.
ADVANTAGE - Enhances condensing efficiency of micro lens due to different refractive indexes of the micro lens and adhesive agent bonding cover glass on micro lens. Has reduced size due to reduced area for bonding pad and use of **flexible wiring** board as **chip**.
DESCRIPTION OF DRAWING(S) - The figure shows the side sectional view of the **solid-state image** pick-up.
Chip 2
Cover glass 3
Adhesive agent 4
Micro lens 12
Dwg.3/5

L36 ANSWER 7 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 1999-484687 [41] WPIX
DNN N1999-361716 DNC C1999-142500
TI Metal wiring patterning method used in semiconductor device manufacture for, e.g., **IC**, LSI, **solid state image** pick-up element and LCD apparatus - involves selective dry etching OF metal **wiring layer** of aluminium alloy containing copper , using chlorine and boron tri chloride mixed gas.
DC L03 U11
PA (SONY) SONY CORP
CYC 1
PI JP 11204410 A 19990730 (199941)* 6p
ADT JP 11204410 A JP 1998-6707 19980116
PRAI JP 1998-6707 19980116
AB JP 11204410 A UPAB: 19991011
NOVELTY - A metal **wiring layer** (4) containing mixture of aluminum alloy and copper is formed on the substrate (1). A layer of photoresist (6) is deposited on the metal layer and a pattern is formed by selective dry etching using a mixed gas of BCl3 and Cl2. The photoresist is ashed using mixed gas which contains hydrogen, sulphur and oxygen.
USE - In manufacture of semiconductor device such as **IC**, LSI, CCD and LCD apparatus.
ADVANTAGE - Produces a reliable semiconductor device with high quality since generation of pitting corrosion by metal wiring corrosion is avoided. Raises electromigration resistance as wiring reliability is increased, thus improving the durability and reliability of semiconductor device.
DESCRIPTION OF DRAWING - The figure shows the wiring patterning method in semiconductor device manufacture. (1) Substrate; (4) Metal **wiring layer**; (6) Photoresist.
Dwg.1/10

L36 ANSWER 8 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 1994-027518 [04] WPIX
DNN N1994-021326
TI Semiconductor module coupled to pcb by face-down technology - has contact bumps of solder for connecting **chip** electrodes to circuit board

electrodes, with wall piece not in contact with bumps.
DC U11 U13 V04 X24
IN KONDOH, Y; SAITO, M; TOGASAKI, T
PA (TOKE) TOSHIBA KK
CYC 3
PI DE 4323799 A1 19940120 (199404)* 18p
JP 06037143 A 19940210 (199411)
US 5448114 A 19950905 (199541) 16p
ADT DE 4323799 A1 DE 1993-4323799 19930715; JP 06037143 A JP 1992-188308 19920715; US 5448114 A Cont of US 1993-91187 19930714, US 1995-389743 19950215
PRAI JP 1992-188308 19920715
AB DE 4323799 A UPAB: 19940307
On the circuit board (2) several electrodes (8) are formed, corresp. to the **chip** electrodes (5). Several contact bumps (4) couple the chip electrodes to the circuit board ones on a 1:1 basis, with the bumps formed by solder metal. A wall element (2) of solder metal, not touching the contact bumps, connects the **chip** surface to that of the circuit board.

Pref. the same metal is used for the wall element and the contact bumps. A first coupling layer (6) of the **chip** electrode material is provided between the **chip** (1) and the all element, while a second coupling layer (7) of the board electrode material is provided between the circuit board and the wall element.

USE/ADVANTAGE - For face-down **chip** mounting in CCD camera etc., insensitive to thermal stress.
Dwg.1/21

L36 ANSWER 9 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 1992-387302 [47] WPIX
TI **Solid-state image** sensor - has sensor **chip** secured on transparent carrier and wired to conductor patterns on flexible film bonded to carrier NoAbstract.
DC U13 W02
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 04287370 A 19921012 (199247)* 6p <--
ADT JP 04287370 A JP 1991-52083 19910318
PRAI JP 1991-52083 19910318

L36 ANSWER 10 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 1991-134299 [19] WPIX
DNN N1991-103191
TI Package for **solid state** imaging circuit - has **chip** package in container receiving visible light sandwiched between plates of high insulation and matched expansion.
DC U12 U13 W04
IN HATTA, M
PA (MITQ) MITSUBISHI DENKI KK
CYC 5
PI EP 425776 A 19910508 (199119)*
R: DE FR GB
JP 03145745 A 19910620 (199131)
US 5087964 A 19920211 (199209)
EP 425776 B1 19940427 (199417) EN 17p
R: DE FR GB
DE 69008480 E 19940601 (199423)
ADT EP 425776 A EP 1990-114971 19900803; US 5087964 A US 1990-561578 19900802; EP 425776 B1 EP 1990-114971 19900803; DE 69008480 E DE 1990-608480 19900803, EP 1990-114971 19900803
FDT DE 69008480 E Based on EP 425776

PRAI JP 1989-285224 19891031
AB EP 425776 A UPAB: 19930928
The semiconductor has a semiconductor **chip** (14) packaged in a semiconductor container which operates in receiving visible light near infrared and ultraviolet light. The package includes a lower plate (11) formed of a material which hardly transmits light with high insulation resistance and high mechanical intensity and has coefficient of expansion close to the **chip**.

A middle plate comprises a wiring board and upper plate (16) is formed with the same parameters of upper plate and has a window (22) for incident light and the whole sealed of glass or synthetic resin.

USE/ADVANTAGE - Could be used for space environment e.g. artificial satellite. Internal stress is low and reliability is high.
3/18

L36 ANSWER 11 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 1986-208560 [32] WPIX
TI **Solid state image** pick-up device mfr. - by integrating driver circuit on **wafer** and depositing metal oxide on **wiring layer** of aluminium silicon-copper
NoAbstract Dwg 3/3.
DC L03 U13
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 61141173 A 19860628 (198632)* 2p
ADT JP 61141173 A JP 1984-263365 19841213
PRAI JP 1984-263365 19841213

L36 ANSWER 12 OF 31 WPIX (C) 2002 THOMSON DERWENT
AN 1984-277338 [45] WPIX
DNN N1984-207025
TI **Solid-state** imaging device having colour filter array structure - is integrally formed on sensor surface as focussing portions in one-to-one correspondence with several picture elements.
DC P81 P84 U11 U13 W04
IN MIYAMURA, M; TAKEMURA, Y; TAKIZAWA, Y
PA (TOKE) TOSHIBA KK
CYC 6
PI EP 124025 A 19841107 (198445)* EN 20p
R: DE FR GB NL
JP 59198754 A 19841110 (198451)
US 4721999 A 19880126 (198807)
EP 124025 B 19910724 (199130)
R: DE FR GB NL
DE 3484828 G 19910829 (199136)
ADT EP 124025 A EP 1984-104409 19840418; JP 59198754 A JP 1983-72104 19830426; US 4721999 A US 1984-602689 19840423
PRAI JP 1983-72104 19830426
AB EP 124025 A UPAB: 19930925
The device has several picture elements (pel) e.g. photodiodes (12) formed on a semiconductor substrate (11) in a 2-0 array. Transfer sections (13) are formed between every two adjacent pels. A **solid state image** sensor (19) is constituted by two polysilicon **wiring layers** (15,16).- On an upper surface of a base layer (17) a colour filter array (18), comprising a full colour light transmitting filter (W), red light cutoff filter (C) and blue light cutoff filter (Y), is formed.

These filter portions constitute focusing sections (10) and are aligned w.r.t. to the pels in a one-to-one correspondence. Each focussing section has a convex lens shape.

USE/ADVANTAGE - Single **chip** colour camera. Has high

spectral response or sensitivity, performing correct colour signal sepn. for good **image** quality.
1/10

L36 ANSWER 13 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 2002-100751 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN MATSUKI YASUHIRO
PA CANON INC
PI JP 2002100751 A 20020405 Heisei
AI JP 2000-287207 (JP2000287207 Heisei) 20000921
PRAI JP 2000-287207 20000921
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide a small and thin **solid-state image** pickup device where an imaging characteristics and reliability are maintained.
SOLUTION: The **solid-state image** pickup device is provided where a **solid- state** imaging element **chip** electrically connected to a **flexible wiring** board comprising an insulating film and a conductor wiring is bonded to a translucent optical glass cap provided on the **image** pickup element surface side of the **solid-state image** pickup element **chip**, with the **solid-state image** pickup **chip** and the outer perimeter of the optical glass cap sealed up with sealing resin. A preventing resin layer, comprising a resin whose linear expansion coefficient being equal to or above the optical glass cap, is provided to the rear surface side of the **solid-state image** pickup element **chip**.
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L36 ANSWER 14 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 2002-076322 JAPIO
TI **SOLID-STATE** IMAGING DEVICE AND MANUFACTURING METHOD
IN OKABE KOJI; MORI HIROYUKI
PA SONY CORP
PI JP 2002076322 A 20020315 Heisei
AI JP 2000-262378 (JP2000262378 Heisei) 20000831
PRAI JP 2000-262378 20000831
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To reduce the tilt of the forming face of an on-**chip** lens at the peripheral edge of an **image** pickup part and to improve **image** quality.
SOLUTION: A **solid-state** imaging device has an **image** pickup part 2 including a light receiving part 5 and a vertical transfer part 7 formed on a substrate; and transfer electrodes 10a, 10b, 11a and 11b on which transfer clock signals ϕV1, ϕV2, ϕV3 and ϕV4 are applied when transferring a signal charge formed on the vertical transfer part 7, generated in the light receiving part 5, and swept out to the vertical transfer part 7. Clock **wiring layers** 12a, 12b, 12c and 12d connected to the transfer electrodes 10a to 11b are wired at the periphery of the **image** pickup part 2. The thickness t2 of first conduction layers (12a to 12d and 13) including the clock **wiring layers** is thinner than the thickness t1 of second conduction layers (electrode pads 14, for example) which are in the same hierarchy as the first conduction layers, are constituted of the same material and are outer than the first conduction layers.
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L36 ANSWER 15 OF 31 JAPIO COPYRIGHT 2002 JPO

AN 2001-196571 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN TANIGAWA KOICHI
PA SONY CORP
PI JP 2001196571 A 20010719 Heisei
AI JP 2000-1160 (JP2000001160 Heisei) 20000107
PRAI JP 2000-1160 20000107
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To reduce the step on the boundary of the effective **image** pickup region and the non-**image** pickup region of a **solid-state image** pickup device.
SOLUTION: Insulating films 120 and 121 are formed on a non-**image** pickup region 100B of a semiconductor **chip** 100 and recessed parts 126 are formed in the upper surface of the **film** 121. **Wiring films** 123A to 123D are arranged in these recessed parts 126. Moreover, recessed parts 128 are formed on the upper surface of the film 121. Hereby, as steps due to the films 123a to 123D and a light-shielding film 125 on the peripheral parts of an effective **image** pickup region 100A of the **chip** 100 can be reduced, further planarizing of the surface of the **chip** 100 becomes possible in comparison with the conventional structure of the **chip** 100. As this result, light which is transmitted on-**chip** lenses 140 and color separation filters 130 and is made incident in a region 100A, can be properly fed to photosensors 111 which constitutes imaging pixels and the uniformity of the sensitivity and color of the light and the like can be modified.

L36 ANSWER 16 OF 31 JAPIO
AN 2001-016486 JAPIO
TI **SOLID-STATE** IMAGING DEVICE MODULE
IN HIRAI HIROYUKI; FUKUOKA YOSHITAKA
PA TOSHIBA CORP
PI JP 2001016486 A 20010119 Heisei
AI JP 1999-180774 (JP11180774 Heisei) 19990625
PRAI JP 1999-180774 19990625
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide an extremely small **solid-state** imaging device module corresponding to high **image** quality with an inexpensive production cost and simple structure.
SOLUTION: In the module, a CCD ship 4 is mounted by inner read bonding at a position corresponding to the device hole 2 of a polyimide **wiring film**, and passive parts 6 such as a semi-conductor **chip** 5 or a **chip** resistance are mounted and loaded on the same **wiring film**. Then the **wiring film** where a plurality of **chip** parts are mounted and loaded is bent with a part mounting surface as an inner side, shaped to be a cylindrical shape and kept in shape and insulated by a resin packed layer 12 such as an epoxy resin.

L36 ANSWER 17 OF 31 JAPIO
AN 2000-209472 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN MIYASHITA TAKETO; KAJINAMI HITOSHI; SUZUKI YASUYUKI
PA SONY CORP
PI JP 2000209472 A 20000728 Heisei
AI JP 1999-4567 (JP11004567 Heisei) 19990111
PRAI JP 1999-4567 19990111
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide a **solid-state**

image pickup device capable of miniaturizing an **image** pickup unit and further narrowing and shortening the hardened tip part of an endoscope or the like.
SOLUTION: The **image** pickup unit is constituted of an unpackaged **solid- state image** pickup **chip** 18 and a circuit board 20 connected to the back surface side where an electronic component 19 is mounted and a bonding pad 25 provided on the **solid-state image** pickup **chip** 18 and the bonding pad 27 provided on one surface of the circuit board 20 are electrically connected by a connection means 30 composed of a **film** where a **wiring** pattern is formed. The electronic component 19 is turned to a hidden state and mounted to a recess 28 formed on the end face of the circuit board 20, the surface of the circuit board 20 orthogonal to the surface provided with the connection means 30 is lower than the outer shape of the **solid-state image** pickup **chip** 18 and a level difference part 26 is formed. The level difference part 26 is provided with a terminal part 29 for connecting a signal cable 31 and the electronic component 19 mounted together with the circuit board 20 and the terminal part 29 of the signal cable 31 are settled within the projection area of the **solid-state image** pickup **chip** 18.

L36 ANSWER 18 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 2000-199863 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN MIYASHITA TAKETO; KAJINAMI HITOSHI; SUZUKI YASUYUKI
PA SONY CORP
PI JP 2000199863 A 20000718 Heisei
AI JP 1999-2094 (JP11002094 Heisei) 19990107
PRAI JP 1999-2094 19990107
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To obtain a **solid-state image** pickup device which enables the miniaturization of an **image** pickup unit and is capable of additionally reducing the diameter at the front end of an electronic endoscope, etc.
SOLUTION: Bonding pads 25 disposed at the outer peripheral part of a **solid-state image** pickup **chip** 18 and bonding pads 26 disposed at a perpendicularly facing substrate 20a bonded to the rear surface of the **solid-state image** pickup **chip** 18 are connected by a connecting means 29 consisting of a **film** formed with **wiring** patterns. The rear surface of the substrate 20a is joined with a horizontally facing substrate 20b. Electronic parts 19 are packaged to the stepped surface of the substrate 20b recessed from the substrate 20 and signal cable 30 are connected to the terminal parts 27 formed at the end of the stepped surface of the substrate 20b. As a result, the substrate 20 and 20b, the electronic parts 19 packaged at the substrate 20b and the terminal parts 27 of the signal cables are housed within the projection area of the **solid-state image** pickup **chip** 18.

L36 ANSWER 19 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1999-271646 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE FOR ELECTRONIC ENDOSCOPE
IN NISHIMURA YOSHIRO
PA OLYMPUS OPTICAL CO LTD
PI JP 11271646 A 19991008 Heisei
AI JP 1998-92208 (JP10092208 Heisei) 19980323
PRAI JP 1998-92208 19980323

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a **solid-state image** pickup device capable of being miniaturized and reducing a cost without lowering work efficiency.
SOLUTION: A through-hole 8 is provided on the end part of a flexible substrate 1 loaded with a **solid-state image** pickup element 2, a semiconductor element 3 and a **chip** component 4 and the **coated** core **wire** 10 of an external signal line 5 with a shield part is passed through the through-hole 8 of the substrate 1 and electrically connected and fixed to a wiring pattern 1a provided on one surface of the substrate 1 by solder 21. Further, the shield part of the external signal line 5 is electrically connected and fixed to the wiring pattern 1b at the through-hole peripheral part of the other surface of the substrate 1 by the solder 21, the external signal line with the shield part is connected by using both surfaces of the flexible substrate 1 and the miniaturization is performed.
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L36 ANSWER 20 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1998-004510 JAPIO
TI CAMERA
IN IKEDA SHIGEO
PA SONY CORP
PI JP 10004510 A 19980106 Heisei
AI JP 1996-155234 (JP08155234 Heisei) 19960617
PRAI JP 1996-155234 19960617
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To make the camera small even when lots of peripheral circuits are provided by providing an **IC chip** and / or other electronic components being peripheral circuits of a **solid-state image** pickup element in an inner face of a light shield case.
SOLUTION: A lens 7 is placed so as to form the **image** of an object to a **solid-state image** pickup element 3 and adhered to a base 1 by an adhesives 9. The light shield case 10 has an opening 11 and it is closed by an optical filter 12 and a lower face is adhered to a peripheral part of the base 1. A **wiring film** 13 is formed in the inner face of the case 10 and an **IC chip** 4 is mounted to a part in contact with a ceiling. Naturally other electronic component than the **IC chip** may be mounted on this part. An external terminal 20 formed to a side face of the case 10 is a part to be connected to the outside of the **wiring film** 13 and connected to an extended part of the **wiring film** 13 to attain electronic continuity. Thus, since the **IC chip** 4 is provided to the inner face of the case 10, the inner space formed by the board 1 and the case 10 is effectively utilized.
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L36 ANSWER 21 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1996-307743 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN KIMURA MASANOBU; SEGAWA MASAO; SUGI SHUICHI
PA TOSHIBA CORP
TOSHIBA AVE CORP
PI JP 08307743 A 19961122 Heisei
AI JP 1995-106325 (JP07106325 Heisei) 19950428
PRAI JP 1995-106325 19950428
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To easily make a camera head thin in diameter, to facilitate assem bling work and to accurately obtain an optical axis.

CONSTITUTION: An **image** pickup element module 200 is constituted in such a way that an optical filter 201 and a **solid-state image** pickup element **chip** 202 are arranged on one and another sides of a flexible board, and one terminal of a supporting base 203 is fixed, and a rigid circuit board 204 is provided on the other terminal side of the supporting base 203, and the pattern **wiring** of the **flexible** board is connected electrically to that of the circuit board by displacing the flexible board along the supporting base. A lens side outside case 113 is provided with a receiving part on which the tip of the optical filter 201 is abutted when the **image** pickup element module 200 is inserted from a rear hollow part. An intermediate outside case chassis 114 is integrated with the lens side outside case 113 with screw structure, and houses the circuit board part by pressing the rear terminal part of the supporting base, and also, into which the tip of a camera cable is inserted from the rear terminal part.

L36 ANSWER 22 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1996-227984 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN HOKARI YASUAKI
PA NEC CORP
PI JP 08227984 A 19960903 Heisei
AI JP 1995-32173 (JP07032173 Heisei) 19950221
PRAI JP 1995-32173 19950221
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To enable reduction in size of an **image** pickup camera and saving of fabrication cost by mounting as compact as possible a **solid state image** pickup element **chip** on a printed wiring board.
CONSTITUTION: A resin package frame 12 and a package board 13 are provided sandwiching a **flexible** printed **wiring** substrate 22 and are then integrally formed. An **image** pickup element **chip** 1 is bonded and fixed on the surface within the package frame 12. A bonding pad 32 of the element **chip** 1 is connected, by the bonding wire 5, with the part within the package frame 12 in the wiring pattern 24 of the printed wiring substrate 22. The part outside the package frame 12 within the wiring pattern 24 becomes the connecting wiring for the other mounting parts such as **IC** and also becomes the connecting electrode for mounting these parts. When the substrate 22 is bent to the rear surface side after the other mounting parts are mounted in the rear surface side of the printed wiring substrate 22, the mounted parts are located at the lower part of the package board 13. Thereby, the **solid-state image** pickup, apparatus can be accommodated in contact into a camera housing.

L36 ANSWER 23 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1992-207072 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN KONDO TAKESHI; SAITO MASAYUKI
PA TOSHIBA CORP
PI JP 04207072 A 19920729 Heisei
AI JP 1990-340334 (JP02340334 Heisei) 19901130
PRAI JP 1990-340334 19901130
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992
AB PURPOSE: To prevent a sealing resin from flowing onto a picture element by forming a conductor pattern on a light-transmission substrate at a region along an outer side around a picture element area so that a distance between adjacent patterns is shorter than a specified distance.

CONSTITUTION: A bump 4 is formed at a portion which is in contact with an electrode pad of a **solid-state image** pickup element **chip** 1 and the **solid-state image** pickup element **chip** 1 is electrically connected to an electrode pattern 5 via the bump 4. A resin is intercepted at a portion where the bump 4 exists. Furthermore, soaking of resin is obstructed by surface tension between bumps (0.5mm max.) and where a thick **film wiring** exists. Also, conditions for preventing a sealing resin from entering an light-receiving area of the sealing resin are formation of a conductor pattern at 60% or more periphery of the entire periphery along an outer periphery around a picture element area of the **solid-state image** pickup element **chip** and a thickness of the conductor pattern being equal to 10% or more of a distance from surface of a light- transmission substrate to the **solid-state image** pickup element **chip**

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L36 ANSWER 24 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1991-211769 JAPIO
TI **SOLID-STATE IMAGE** SENSOR/AMPLIFIER
IN KAIDA MASUMI; NISHIZAWA SHIGEKI; TAKEMOTO KAYAO
PA HITACHI LTD
PI JP 03211769 A 19910917 Heisei
AI JP 1990-6132 (JP02006132 Heisei) 19900117
PRAI JP 1990-6132 19900117
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1991
AB PURPOSE: To provide an imaging device with an additional capacitor array by forming a double-**layer wiring** structure for pixel signal read lines to utilizing capacitance between layers, so that capacitors can be incorporated within a **chip** without making the **chip** size larger.
CONSTITUTION: Column signal lines V1-V3 are connected to first ends of capacitors CV1-CV3, respectively. The second ends of these capacitors are connected through switching MOSFETs Q20-Q22 and a lateral control line to a terminal CRV. The second end of the capacitor CV1 is connected through switching MOSFETs Q23 and Q24 to first ends of capacitors CS1 and CS2. The second ends of these capacitors CS1 and CS2 connected to the terminal CRV through the control line. Signal lines are formed in a double-**layer wiring** structure having insulator or dielectric between two layers. Therefore, capacitors are formed between pixel signal lines without making the **chip** size larger.

L36 ANSWER 25 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1991-145745 JAPIO
TI SEMICONDUCTOR DEVICE
IN HATTA MUNEO
PA MITSUBISHI ELECTRIC CORP
PI JP 03145745 A 19910620 Heisei
AI JP 1989-285224 (JP01285224 Heisei) 19891031
PRAI JP 1989-285224 19891031
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1991
AB PURPOSE: To lessen the warpage of the surface of a semiconductor **chip** and to reduce an internal stress in the **chip** by a method wherein silicon carbide or Al nitride is used as the material for lower and upper plates, the semiconductor **chip** is mounted on the lower plate, a middle plate is bonded on the **chip** by the upper and lower plates holding the middle plate consisting of a single layer or a plurality of **layers** of a **wiring** board between the upper and lower plates, the upper part of the frame of the upper plate is

sealed by a cap body consisting of glass or a synthetic resin and light is incident through an opening part provided in the upper plate.
CONSTITUTION: An **image** sensor **chip** 14 consisting of a **solid-state image** sensing element made of silicon and the like has pads 15 and is bonded on a lower plate 11. A rectangle-shaped hole 22 for light incidence use is provided in an upper plate 16. After the plates 11 and 16 are formed into a plate having a flatness of 20 to 50μm or thereabouts all over the surface of the plate, a glass cover 18 and the plate 16, the plate 16 and a middle plate 12, the plate 12 and the plate 11 and the **chip** 14 and the plate 11 are respectively adhered and bonded with a solder or a bonding agent consisting of a resin or the like. The plates 11 and 116 are both formed of silicon carbide, whose linear expansion coefficient is very approximate to that of silicon constituting the **chip** 14.

L36 ANSWER 26 OF 31 JAPIO
AN 1991-027684 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE
IN OGATA MASAKI
PA OLYMPUS OPTICAL CO LTD
PI JP 03027684 A 19910206 Heisei
AI JP 1989-160897 (JP01160897 Heisei) 19890626
PRAI JP 1989-160897 19890626
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1991
AB PURPOSE: To reduce the **chip** area by forming a horizontal scanning circuit and a vertical scanning circuit along one and the same side of an **image** area respectively.
CONSTITUTION: A horizontal scanning circuit 32 and a vertical scanning circuit 33 are arranged along sides 31a, 31b of an **image** area 31 opposite to each other, the circuit 32 connects to a source line 19 and the circuit 33 connects to a gate line selection line 23 via a contact 34. Then a thin film 35 to shield the light is provided to the scanning circuits 32, 33. When the wiring in the circuit 33 is formed by using a 2-**layer wiring** made of metallic thin films of 1st and 2nd layers, the contact 34 connects an output wire for the circuit 33 of the 2nd layer metallic thin film and the line 23 of the 3rd layer metallic thin film. Thus, the longitudinal and lateral size of the **solid-state image** pickup element is reduced by the width of the scanning circuits and the **chip** area is reduced.

L36 ANSWER 27 OF 31 JAPIO
AN 1988-148226 JAPIO
TI ENDOSCOPE
IN FUKUOKA YOSHITAKA
PA TOSHIBA CORP
PI JP 63148226 A 19880621 Showa
AI JP 1986-296169 (JP61296169 Showa) 19861212
PRAI JP 1986-296169 19861212
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To improve resolution and to prolong file by composting an **image** pickup means of an **image** pickup element and beveling the periphery of a **chip** carrier which is close to the inner peripheral surface of an envelope and extends in the axial direction of the envelope.
CONSTITUTION: The **solid-state image** pickup element 8 is mounted on the **chip** carrier 7 and covered with a metallic cap with a glass window which is made of glass or transparent sapphire, etc., for sealing the **solid-state image** pickup element 8 airtightly. Then the **image** pickup

means 6 is fixed on a **flexible wiring** board 12 where circuit elements 11 such as plural decoupling capacitors are mounted, and the joining part between the **chip** carrier 7 and **flexible wiring** board 12 is sealed with organic insulating resin 13. The **chip** carrier 7 is a rectangular body made of a ceramic base body such as alumina and the periphery of the **chip** carrier 7 which is close to the inner peripheral surface of the envelope 2 and extends in the axial direction of the envelope 2 is beveled. Consequently, the resolution is high, the life is long, and **image** information can be led out as a television signal.

L36 ANSWER 28 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1988-147131 JAPIO
TI ENDOSCOPE
IN FUKUOKA YOSHITAKA
PA TOSHIBA CORP
PI JP 63147131 A 19880620 Showa
AI JP 1986-295380 (JP61295380 Showa) 19861211
PRAI JP 1986-295380 19861211
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To improve the resolution of an endoscope, to prolong its life, and to output **image** information as a television signal by sealing a **solid-state image** pickup element which constitutes an **image** pickup means airtightly with a metallic cap which has a transparent window and forming this metallic cap and a metallic frame in one body.
CONSTITUTION: The metallic cap 9 with the glass window which covers the state **image** pickup element 8 mounted on a **chip** carrier 7 airtightly is arranged. Further, the metallic frame 10 is formed integrally along the outer periphery of the metallic cap 9 with the glass window. This **image** pickup means 6 is fixed on a **flexible wiring** board 12 where circuit elements 11 such as a transistor, plural resistance **chip**, plural decoupling capacitors, etc., forming an emitter follower circuit for the impedance conversion of the **image** pickup signal from the **solid-state image** pickup element 8 are mounted. Then the joint part between the **chip** carrier 7 and **flexible wiring** board 12 is sealed with organic resin 13. Consequently, the resolution is high, the life is prolonged, and the **image** information is led out as the television signal.

L36 ANSWER 29 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1988-147130 JAPIO
TI ENDOSCOPE
IN FUKUOKA YOSHITAKA
PA TOSHIBA CORP
PI JP 63147130 A 19880620 Showa
AI JP 1986-295379 (JP61295379 Showa) 19861211
PRAI JP 1986-295379 19861211
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To shorten the overall length of an envelope, i.e. its tip hard part and to facilitate observing operation by mounting a circuit element which processes a video signal from a **solid-state image** pickup element on a **chip** carrier.
CONSTITUTION: A **flexible wiring** board 12 is reduced in width at its position where the **chip** carrier is mounted and increased in width from the position where the circuit element 11 is mounted toward the rear. A bare **chip** Tr and plural resistance **chips** R which form an emitter follower circuit for the impedance

conversion of the **image** pickup signal from the **solid-state image** pickup element 8 are mounted on the **chip** carrier 7. The flexible board 12 is shortened in overall length as compared with a product having said elements mounted on a small-sized **chip** components. Consequently, the overall length of the envelope, i.e. tip hard part becomes short, he radius of rotation of this envelope is reduced, and the expansion of a doctor's observation range, and diagnoses and treatments by a doctor are facilitated.

L36 ANSWER 30 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1985-145656 JAPIO
TI **SOLID-STATE IMAGE** PICKUP DEVICE AND MANUFACTURE THEREOF
IN GOTO HIROSHIGE
PA TOSHIBA CORP
PI JP 60145656 A 19850801 Showa
AI JP 1984-1660 (JP59001660 Showa) 19840109
PRAI JP 1984-1660 19840109
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1985
AB PURPOSE: To reduce the number of steps in the bonding process by reducing the number of wires between an element **chip** and the casing by a method wherein the pad part of a specific **wiring** conductive **film** and the pad part of a photo shielding conductive film are connected to the casing by means of a common bonding wire.
CONSTITUTION: The pad part 16' of the photo shielding conductive film 12' is formed by superposition on the pad part 14' of the conductive film 13' of the **wiring** conductive **films** 13... for a linear sensor **chip** 10, which is to be set at the same potential as that of the conductive film 12' formed around a photosensitive region 11. This pad part 16' is connected to the metallized part 21 of the casing 20 by means of a bonding wire 17. The pad part 16' is connected to the pad part 14' by pressure bonding by the bonding press-contact force on the pad part 16'. The pad parts 16' and 14' can be connected to the metallized part 21 by means of a piece of bonding wire 17, thus reducing the number of wires.

L36 ANSWER 31 OF 31 JAPIO COPYRIGHT 2002 JPO
AN 1984-139672 JAPIO
TI **SOLID-STATE IMAGE** PICKUP ELEMENT
IN KOIKE NORIO; TSUKADA TOSHIHISA; UMAJI TORU; ANDO HARUHISA
PA HITACHI LTD
PI JP 59139672 A 19840810 Showa
AI JP 1984-7128 (JP59007128 Showa) 19840120
PRAI JP 1984-7128 19840120
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AB PURPOSE: To obtain a two-storied **image** pickup element which can be formed at the minimum processes of manufacture by a method wherein an insulating oxide film is formed on the upper part of a scanning **IC** substrate, the oxide film on the specific junction region of an MOS transistor is removed, and a two-dimensional electrode pattern to be used for formation of a picture element conductive to the junction part is formed on the upper part of the junction region.
CONSTITUTION: After a gate, a source junction and a drain junction have been formed, an oxide film 18 to be used for insulation is formed. Subsequently, the oxide film 18 located on the desired source or drain is removed by performing a photo etching, and a metal film is vapor-deposited. A scanning **IC** substrate 21, whereon a scanning circuit on a semiconductor substrate and a switch 20 for positional selection are integrated, is formed. An electrode 24 with which the unit measurements of photoelectric conversion, a picture element in other

words, will be determined is formed. This electrode is the second **layer** for the **wiring** 19, the ohmic contact with the junction of an MOS switch can be maintained through a contact hole 19, and the above is electrically isolated from the first **layer** **wiring** 19 by an insulating film 22.

12/20/2002

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Set	Items	Description
S1	1217	AU=(MOCHIZUKI, KATSUHISA OR MOCHIZUKI KATSUHISA OR MOCHIZUKI, K)
S2	1301200	DIE OR CHIP? ? OR IC OR ICS OR MICRO(W)CHIP? ? OR MICROCHIP? ? OR MICROCIRCUIT? ? OR MICRO(W)CIRCUIT? ? OR DICE OR WAFER? ? OR INTEGRATED(W)CIRCUIT? ? OR LOGIC(W)CIRCUIT? ?
S3	72660	CC=B2570 Semiconductor integrated circuits
S4	271416	ELECTRICAL?(2N)CONDUCT?
S5	15488	ELECTRICAL?(2N)(CONNECT? OR JOIN? OR LINK? OR CONJOIN?)
S6	12903	WIR???(2N)(FILM? OR LAYER? OR COAT? OR FLEXIBLE OR ELASTIC OR FLEXILE OR SPRINGY OR FLEXUOUS)
S7	680874	CIRCLE? OR OVAL? OR SPHERE? ? OR CIRCULAR
S8	551038	SOLID(W)STATE
S9	1630418	IMAGE? ?
S10	912659	LEAD (January 1969)
S11	25	S1 AND (S2:S3)
S12	21	RD (unique items)
S13	1310619	S2:S3
S14	24	S6 AND S10 AND S4
S15	24	S14 NOT S11
S16	22	RD (unique items)
S17	30	S13 AND S5 AND S6
S18	29	S17 NOT (S11 OR S14)
S19	21	RD (unique items)
S20	3	S13 AND S5 AND S8 AND S9
S21	63	S13 AND S5 AND S8
S22	0	S21 AND S7
S23	8	S21 AND S10
S24	10	(S23 OR S20) NOT (S11 OR S14 OR S17)
S25	9	RD (unique items)
S26	19842	S8 AND S9
S27	10	S26 AND S6
S28	392	S26 AND S10
S29	93	S28 AND S13
S30	1	S28 AND ELECTRIC?(2N)CONDUCTOR?
S31	9	S28 AND S7
S32	11	S28 AND (INSULAT? OR OXIDE OR DIELECTRIC)(2N)(FILM? OR COAT? OR LAYER?)
S33	30	(S27 OR S30 OR S31 OR S32) NOT (S11 OR S14 OR S17 OR S23 OR S20)
S34	28	RD (unique items)

12/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10139513 Genuine Article#: 489NN Number of References: 14
Title: A switched-capacitor interface for differential capacitance transducers (ABSTRACT AVAILABLE)
Author(s): Ogawa S (REPRINT) ; Oisugi Y; **Mochizuki K**; Watanabe K
Corporate Source: Shizuoka Univ,Elect Res Inst,Hamamatsu/Shizuoka 432/Japan/ (REPRINT); Shizuoka Univ,Elect Res Inst,Hamamatsu/Shizuoka 432/Japan/; Chiba Precis Corp,Funabashi/Chiba/Japan/; Numazu Coll Technol,Dept Elect Engn,Numazu//Japan/
Journal: IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, 2001, V50, N5 (OCT), P1296-1301
ISSN: 0018-9456 Publication date: 20011000
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: For high-accuracy signal processing of differential capacitance transducers, an interface circuitry based on a switched-capacitor (SC) sample/hold (S/H) circuit is developed. Driven by nonoverlapping two-phase clocks, the interface produces the output voltage which is proportional to the ratio of difference-to-sum of two capacitors of a differential transducer. Performances of a prototype **chip** fabricated using 0.6-mum n-well CMOS process were measured and compared with those simulated by HSPICE. The measured results indicate that 0.1% resolution is achievable with the proposed interface and the temperature-dependence of the interface is small. An interface circuit improved for smaller temperature-dependence is also proposed and its operation is confirmed experimentally.

12/3,AB/2 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10106707 Genuine Article#: 486PQ Number of References: 18
Title: High-speed small-scale InGaP/GaAs HBT technology and its application to **integrated circuits** (ABSTRACT AVAILABLE)
Author(s): Oka T (REPRINT) ; Hirata K; Suzuki H; Ouchi K; Uchiyama H; Taniguchi T; **Mochizuki K**
Corporate Source: Hitachi Ltd,Cent Res Lab,1-280 Higashi Koigakubo/Kokubunji/Tokyo 1858601/Japan/ (REPRINT); Hitachi Ltd,Cent Res Lab,Kokubunji/Tokyo 1858601/Japan/; ULSI Syst Co,Tokyo 1858601//Japan/; Hosei Univ,Dept Elect & Elect Engn,Tokyo 1848584//Japan/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 2001, V48, N11 (NOV), P 2625-2630
ISSN: 0018-9383 Publication date: 20011100
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394 USA
Language: English Document Type: ARTICLE
Abstract: We have developed the advanced performance, small-scale InGaP/GaAs heterojunction bipolar transistors (HBTs) by using WSi/Ti base electrode and buried SiO2 in the extrinsic collector. The base-collector capacitance C-BC was further reduced to improve high-frequency performance. Improving the uniformity of the buried SiO2, reducing the area of the base electrode, and optimizing the width of the base-contact enabled us to reduce the parasitic capacitance in the buried SiO2 region by 50% compared to our previous devices. The

cutoff frequency f(T) of 156 GHz and the maximum oscillation frequency f(max) of 255 GHz were obtained at a collector current I-C of 3.5 mA for the HBT with an emitter size S-E of 0.5 x 4.5 mum(2), and f(T) of 114 GHz and f(max) of 230 GHz were obtained at I-C of 0.9 mA for the HBT with S-E of 0.25 x 1.5 mum(2). We have also fabricated digital and analog circuits using these HBTs. A 1/8 static frequency divider operated at a maximum toggle frequency of 39.5 GHz with a power consumption per flip-flop of 190 mW. A transimpedance amplifier provides a gain of 46.5 dB . Q with a bandwidth of 41.6 GHz at a power consumption of 150 mW. These results indicate the great potential of our HBTs for high-speed, low-power circuit applications.

12/3,AB/3 (Item 3 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10089398 Genuine Article#: 484EL Number of References: 28
Title: Characterization of InGaP/GaAs heterojunction bipolar transistors with a heavily doped base (ABSTRACT AVAILABLE)
Author(s): Oka T (REPRINT) ; Ouchi K; **Mochizuki K**
Corporate Source: Hitachi Ltd,Cent Res Lab,1-280 Higashi Koigakubo/Kokubunji/Tokyo 1858601/Japan/ (REPRINT); Hitachi Ltd,Cent Res Lab,Kokubunji/Tokyo 1858601/Japan/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 2001, V40, N9A (SEP), P5221-5226
ISSN: 0021-4922 Publication date: 20010900
Publisher: INST PURE APPLIED PHYSICS, DAINI TOYOKAIJI BLDG, 4-24-8 SHINBASHI, MINATO-KU TOKYO, 105-004, JAPAN
Language: English Document Type: ARTICLE
Abstract: Characteristics of InGaP/GaAs heterojunction bipolar transistors (HBTs) with a heavily doped base are examined at the base doping level N-B ranging from 5 x 10(19) to 5 x 10(20) cm(-3). At N-B of less than 3 X 10(20) cm(-3), the current gain is mainly determined by Auger recombination in the intrinsic base region and is inversely proportional to the square of N-B. In contrast, the current gain at N-B above 3 x 1020 cm(-3) is significantly decreased. We evaluated the effective barrier height of holes between the emitter and the base by measuring temperature dependence of current gain, and found that the effective hole barrier is reduced as N-B increases. This result is explained by the large energy shift of the Fermi level inside the valence band due to heavy doping, causing the increase in the back injection of holes into the emitter, and thus reducing the current gain.

12/3,AB/4 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

09749967 Genuine Article#: 443RW Number of References: 66
Title: Imaging evaluation of the cirrhotic liver (ABSTRACT AVAILABLE)
Author(s): Murakami T (REPRINT) ; **Mochizuki K**; Nakamura H
Corporate Source: Osaka Univ,Grad Sch Med, Dept Diagnost Med Radiol,2-2 Yamadaoka/Suita/Osaka 5650871/Japan/ (REPRINT); Osaka Univ,Grad Sch Med , Dept Diagnost Med Radiol,Suita/Osaka 5650871/Japan/; Osaka Univ,Grad Sch Med, Dept Internal Med & Therapeut,Suita/Osaka 5650871/Japan/
Journal: SEMINARS IN LIVER DISEASE, 2001, V21, N2 (MAY), P213-224
ISSN: 0272-8087 Publication date: 20010500
Publisher: THIEME MEDICAL PUBL INC, 333 SEVENTH AVE, NEW YORK, NY 10001 USA
Language: English Document Type: REVIEW

Abstract: Because recent advances in medical care decrease the mortality rate due to liver cirrhosis itself, many cirrhotic patients **die** due to hepatocellular carcinoma. Accordingly, the role of radiology in the evaluation of the patient with cirrhosis is primarily to characterize the morphologic manifestations of the disease, evaluate the hepatic and extrahepatic vasculature, assess the effects of portal hypertension, and detect hepatic tumors. When the latter are identified, a critical role of imaging technology is to differentiate hepatocellular carcinoma from other nodular lesions, such as dysplastic nodules and regenerating nodules.

Screening strategies for patients with cirrhosis have been proposed to facilitate the detection of small, asymptomatic hepatocellular carcinomas. Dynamic studies using computed tomography (CT) and magnetic resonance imaging (MRI) are very useful for the diagnosis of hepatic tumors previously detected by ultrasound, as well as for screening. In Japan, patients with documented cirrhosis typically undergo serum alpha-fetoprotein testing and/or PIVKA-II (protein induced by Vitamin K absence or antagonist II) measurements every 2 months, ultrasound every 3 months, and CT or MRI every 6 months. This has resulted in great success in detecting small hepatocellular carcinomas (less than 2 cm in diameter) and early-stage well-differentiated hepatocellular carcinomas.

12/3,AB/5 (Item 5 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08896160 Genuine Article#: 341FL Number of References: 7
Title: GaN/W/W-oxide metal base transistor with very large current gain and power gain (ABSTRACT AVAILABLE)
Author(s): **Mochizuki K (REPRINT)** ; Uesugi K; Asbeck PM; Gotoh J; Mishima T; Hirata K; Oda H
Corporate Source: HITACHI LTD,CENT RES LAB/TOKYO 1858601//JAPAN/ (REPRINT); UNIV CALIF SAN DIEGO,DEPT ELECT & COMP ENGN/LA JOLLA//CA/92093; HITACHI ULSI SYST CORP,/TOKYO 1858601//JAPAN/
Journal: APPLIED PHYSICS LETTERS, 2000, V77, N5 (JUL 31), P753-755
ISSN: 0003-6951 Publication date: 20000731
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501
Language: English Document Type: ARTICLE
Abstract: We demonstrate a GaN/W/W-oxide metal base transistor (MBT) whose collector is formed by oxidizing the intrinsic W base. The thickness of the nonoxidized intrinsic base of the fabricated collector-up MBT on a sapphire substrate was estimated to be 2-3 nm. Although the MBT showed large leakage, subtraction of the leakage from collector cut-rent revealed that the transistor had a very large small-signal direct current (dc) current gain of 87 dB and a de power gain of 50 dB. This indicates that the GaN-based MBT is a possible candidate for microwave and millimeterwave amplifiers as well as for high-speed **integrated circuits** used in optical fiber communication system. (C) 2000 American Institute of Physics. [S0003-6951(00)04231-5].

12/3,AB/6 (Item 6 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

07190336 Genuine Article#: 134QV Number of References: 30
Title: Heavily carbon-doped InGaP/GaAs HBT's with buried polycrystalline

GaAs under the base electrode (ABSTRACT AVAILABLE)
Author(s): **Mochizuki K (REPRINT)** ; Ouchi K; Hirata K; Oka T; Tanoue T
Corporate Source: HITACHI LTD,CENT RES LAB/TOKYO 1858601//JAPAN/ (REPRINT); HITACHI ULSI SYST CO LTD,/TOKYO 1858601//JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1998, V45, N11 (NOV), P 2268-2275
ISSN: 0018-9383 Publication date: 19981100
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: This paper describes a new approach to fabricating InGaP/GaAs heterojunction bipolar transistors (HBT's) with a high cutoff frequency (f(T)) high maximum oscillation frequency (f(max)), and low external collector capacitance (C-bc) To attain a high f(T) and f(max), a heavy carbon-doping (1.3 x 10(20) cm(-3)) technique was used with a thin (30-nm-thick) GaAs base layer, while for low C-bc, low-temperature gas-source molecular-beam epitaxial growth on SiO2-patterned substrates was used to bury high-resistance polycrystalline GaAs under the base electrode. An fr of 120 GHz and an f(max) of 230 GHz were achieved for three parallel 0.7 x 8.5 mu m HBT's with an undoped-collector structure, and an fr of 170 GHz and an f(max) of 160 GHz were obtained for a single 0.9 x 10 mu m HBT with a ballistic-collection-transistor structure. Compared to HBT's without buried poly-GaAs, the maximum stable gain was improved by 1.2 dB in the 0.7 x 8.5 mu m HBT and by 23 dB in the 0.9 x 10 mu m HBT due to the reduction in Cbc These results show the high potential of the proposed HBT's for high-speed digital and broadband-amplifier applications.

12/3,AB/7 (Item 7 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06961876 Genuine Article#: 108VJ Number of References: 29
Title: Cross-linking of Fc gamma-receptor on monocytes inhibits hepatitis C virus-specific cytotoxic T-lymphocyte induction in vitro (ABSTRACT AVAILABLE)
Author(s): Kanto T; Hayashi N (REPRINT) ; Takehara T; Katayama K; Ito A; **Mochizuki K**; Kuzushita N; Tatsumi T; Sasaki Y; Kasahara A; Hori M
Corporate Source: OSAKA UNIV,SCH MED, DEPT MED 1, 2-2 YAMADA OKA/SUITA/OSAKA 5650871/JAPAN/ (REPRINT); OSAKA UNIV,SCH MED, DEPT MED 1/SUITA/OSAKA 5650871/JAPAN/
Journal: IMMUNOLOGY, 1998, V94, N4 (AUG), P461-468
ISSN: 0019-2805 Publication date: 19980800
Publisher: BLACKWELL SCIENCE LTD, P O BOX 88, OSNEY MEAD, OXFORD OX2 0NE, OXON, ENGLAND
Language: English Document Type: ARTICLE
Abstract: In hepatitis C virus (HCV) infection, immune complex (**IC**)-type virus particles are frequently observed in circulation. The **IC** leads to cross-linking of Fc gamma receptors (Fc gamma R) on monocytes and exerts immunoinhibitory function. To test the roles of **IC** in HCV-specific cytotoxic T lymphocyte (CTL) induction, we generated HCV CTL from peripheral blood mononuclear cells of chronic hepatitis C patients with or without HCV-**IC**- or immunoglobulin G (IgG)-coated culture plates and compared their lytic activities. HCV-**IC** or adherent IgG, which induces Fc gamma R cross-linking, significantly reduced CTL activity. Expression of B7-1 on monocytes decreased on adherent IgG. In addition, tumour necrosis factor-alpha (TNF-alpha) and transforming growth factor-beta 1 (TGF-beta 1) production increased from cells on adherent IgG and their mRNA expression in monocytes was enhanced. Anti-TNF-a antibody during

induction on adherent IgG inhibited lysis; however, anti-TGF-beta completely reversed its inhibitory effect. These results demonstrated that HCV-**IC** or adherent IgG impaired HCV-CTL induction in vitro. The Fc gamma R-mediated CTL suppression occurred via decreased expression of monocyte B7-1 and/or enhanced production of TGF-beta 1.

12/3,AB/8 (Item 8 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06501280 Genuine Article#: YX447 Number of References: 2
Title: Molecular beam deposition of n-type polycrystalline In0.6Ga0.4As for high resistances in heterojunction bipolar transistor **integrated circuits** (ABSTRACT AVAILABLE)
Author(s): **Mochizuki K (REPRINT)** ; Oka T; Nakamura T
Corporate Source: HITACHI LTD,CENT RES LAB, 1-280 HIGASHI KOIGAKUBO/TOKYO 185//JAPAN/ (REPRINT)
Journal: ELECTRONICS LETTERS, 1997, V33, N13 (JUN 19), P1181-1181
ISSN: 0013-5194 Publication date: 19970619
Publisher: IEE-INST ELEC ENG, MICHAEL FARADAY HOUSE SIX HILLS WAY STEVENAGE, HERTFORD, ENGLAND SG1 2AY
Language: English Document Type: ARTICLE
Abstract: 100nm thick n-type polycrystalline In0.6Ga0.4As layers have been grown on SiO2 by molecular beam epitaxy and their electrical properties have been investigated using Au/Pt/Ti as non-alloyed ohmic metals. A moderate sheet resistance of 4.7 x 10(2) Ohm/square was obtained, together with a low specific contact resistance of 8 x 10(-8) Ohm cm(2). This material should be useful for attaining high resistances in heterojunction bipolar transistor **integrated circuits**.

12/3,AB/9 (Item 9 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06179571 Genuine Article#: YA156 Number of References: 26
Title: Incidence of delayed onset infection after trabeculectomy with adjunctive mitomycin C or 5-fluorouracil treatment (ABSTRACT AVAILABLE)
Author(s): **Mochizuki K (REPRINT)** ; Jikihara S; Ando Y; Hori N; Yamamoto T; Kitazawa Y
Corporate Source: GIFU UNIV,SCH MED, DEPT OPHTHALMOL, 40 TSUKASA MACHI/GIFU 500//JAPAN/ (REPRINT)
Journal: BRITISH JOURNAL OF OPHTHALMOLOGY, 1997, V81, N10 (OCT), P877-883
ISSN: 0007-1161 Publication date: 19971000
Publisher: BRITISH MED JOURNAL PUBL GROUP, BRITISH MED ASSOC HOUSE, TAVISTOCK SQUARE, LONDON, ENGLAND WC1H 9JR
Language: English Document Type: ARTICLE
Abstract: Aims/background-The introduction of the adjunctive use of antiproliferatives to trabeculectomy has greatly improved the success rate of this operation. Trabeculectomy with antiproliferative treatment, however, is usually associated with a cystic and thin walled filtering bleb, which may be more susceptible to infection. The objective of this study was to evaluate the incidence, clinical findings, and risk factors of delayed onset, bleb related infection after trabeculectomy with adjunctive mitomycin C (MMC) or 5-fluorouracil (5-FU) treatment.

Methods-The records of 632 glaucoma patients who underwent 966 trabeculectomies, with and without the use of adjunctive MA **IC** or

5-FU treatment, between January 1985 and February 1995 were analysed. The mean follow up period was 3.5 (2.4) years (range 0.1 to 11.2 years). The mean patient age was 54.8 (18.8) years (range 0 to 88 years).

Results-Bleb related infection occurred in one of 76 trabeculectomies that did not receive antiproliferatives (1.3%), three of 228 treated with 5-FU (1.3%) trabeculectomies, and seven of 662 treated with MMC (1.1%). Five eyes developed blebitis; six eyes developed endophthalmitis. Bleb related infection developed an average of 3.1 (1.6) (range 0.4 to 6.0) years after trabeculectomy. All eyes had avascular or hypovascular blebs that were cystic in shape before infection and all eyes had reduced intraocular pressure. Early wound leaks and chronic, intermittent bleb leaks were identified to be risk factors for the bleb related infection.

Conclusion-The incidence of delayed onset, bleb related infection after trabeculectomy with antiproliferative treatment is similar to that after trabeculectomy without antiproliferatives.

12/3,AB/10 (Item 10 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05055092 Genuine Article#: TM341 Number of References: 18
Title: AN OVERSAMPLING ADC WITH NONLINEAR QUANTIZER FOR PCM CODEC (Abstract Available)
Author(s): SAKIYAMA S; HAYASHI G; DOSHO S; MARUYAMA M; INAGAKI S; MATSUSHITA M; **MOCHIZUKI K**
Corporate Source: MATSUSHITA ELECT IND CO LTD/MORIGUCHI/OSAKA 570/JAPAN/
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 1995, VE78C, N12 (DEC), P 1754-1760
ISSN: 0916-8524
Language: ENGLISH Document Type: ARTICLE
Abstract: This paper describes an oversampling analog-to-digital converter (ADC) suitable far PCM codecs. Nonlinear 5-level quantizer is implemented to noise-shaping modulator. This ADC meets the specifications of ITU-T G.712, in spite of using first order delta-sigma modulator, and realizes low power operation. This **chip** is fabricated in 0.8 mu m double-poly and double-metal CMOS process and occupies a **chip** area of 15 mm(2). Maximum power consumption is 12.8 mW with a single +3 V power supply including DAC and TONE generator.

12/3,AB/11 (Item 11 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02117648 Genuine Article#: KC144 Number of References: 11
Title: ALGAAS/GAAS HBTS FOR 10-GB/S **ICS** USING A NEW BASE OHMIC CONTACT FABRICATION PROCESS (Abstract Available)
Author(s): KUSANO C; MASUDA H; **MOCHIZUKI K**; ISHIKAWA Y; KAWATA M; MITANI K; MIYAZAKI M
Corporate Source: HITACHI LTD,CENT RES LAB/KOKUBUNJI/TOKYO 185/JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1993, V40, N1 (JAN), P25-31
ISSN: 0018-9383
Language: ENGLISH Document Type: ARTICLE
Abstract: A new basic ohmic contact technology for AlGaAs/GaAs heterojunction bipolar transistors (HBT's) has been developed. The

effect of the A]GaAs/GaAs HBT device parameters on the high-frequency performance of HBT **IC**'s for 10-Gb/s systems is analyzed and it is shown that, at a cutoff frequency (f(T)) of 40 GHz or more, reducing base resistance or collector capacitance is more effective than increasing f(T) for obtaining high-frequency performance. A process is developed for fabricating base electrodes with a very-low ohmic contact resistivity, approximately 10(-7) OMEGA . cm2, by using a AuZn/Mo/Au alloy, which provides the required high performance. Self-aligned AlGaAs/GaAs HBT's, with a 2.5 mum X 5 mum emitter, using a AuZn/Mo/Au alloy base metal and an undoped GaAs collector are shown to have a high f(T) and a maximum oscillation frequency of about 45 and 70 GHz, respectively, at 3.5 mA. An AGC amplifier with a 20-dB gain and a bandwidth of 13.7 GHz, which is one of the fabricated 10-Gb/s HBT **IC chip** sets, demonstrates stable performance.

12/3,AB/12 (Item 1 from file: 434)
DIALOG(R)File 434:SciSearch(R) Cited Ref Sci

07102173 Genuine Article#: A0577 Number of References: 6
Title: OBSERVATION OF CHIRP IN A 1.5-MU-M DFB-LD USING A STREAK CAMERA
Author(s): KUWAZURU M; YAMAMOTO S; **MOCHIZUKI K**; FUJISE M
Corporate Source: KDD,RES & DEV LABS,1-23 NAKAMEGURO 2 CHOME,MEGURO KU/TOKYO 153//JAPAN/
Journal: ELECTRONICS LETTERS, 1986, V22, N2, P108-109
Language: ENGLISH Document Type: ARTICLE

12/3,AB/13 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02764847 JICST ACCESSION NUMBER: 96A0101091 FILE SEGMENT: JICST-E
Low-power Analog, Digital LSIs and ASICs for Multimedia. An Oversampling ADC with Non-linear Quantizer for PCM CODEC.
SAKIYAMA S (1); HAYASHI G (1); DOSHO S (1); MARUYAMA M (1); INAGAKI S (1); MATSUSHITA M (2); **MOCHIZUKI K** (2)
(1) Matsushita Electric Industrial Co., Ltd., Moriguchi-shi, JPN; (2) Matsushita Electronics Corp., Kawasaki-shi, JPN
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1995, VOL.E78-C,NO.12, PAGE.1754-1760, FIG.15, TBL.2, REF.18
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.37.037.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes an oversampling analog-to-digital converter (ADC) suitable for PCM codecs. Non-linear 5-level quantizer is implemented to noise-shaping modulator. This ADC meets the specifications of ITU-T G.712, in spite of using first order delta-sigma modulator, and realizes low power operation. This **chip** is fabricated in 0.8.MU.m double-poly and double-metal CMOS process and occupies a **chip** area of 15 mm2. Maximum power consumption is 12.8 mW with a single + 3 V power supply including DAC and TONE generator. (author abst.)

12/3,AB/14 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

12/20/2002

00803099 JICST ACCESSION NUMBER: 89A0005269 FILE SEGMENT: JICST-E
IDTV system high picture quality "S-digital TV".
SUNADA K (1); SATOH H (1); FUJITA S (1); KAWABATA E (1); OKADA Y (1);
MOCHIZUKI K (1); KOGOSHI T (1); SENJU Y (1)
(1) NEC Home Electronics, Ltd., Kawasaki, JPN
NEC Res Dev, 1988, NO.90, PAGE.84-98, FIG.17, TBL.3, REF.4
JOURNAL NUMBER: G0138AAA ISSN NO: 0547-051X CODEN: NECRA
UNIVERSAL DECIMAL CLASSIFICATION: 621.397.62
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The C-29D70 is a 29-inch high picture quality S-digital TV based on the IDTV(Improved Definition TV) system and incorporates the industry's first 3-dimensional digital filter in its video signal processing circuit; the result of NEC's LSI and digital technology. For improved picture quality, the C-29D70 uses seven newly developed dedicated LSI **chips** (Y-C separation, Y-C processing, Y-C interpolation, chrominance demodulation, movement detection, clock generation, noise reducer) and an image field buffer. Major improvements in picture quality include the elimination of line flicker and line crawling, higher vertical resolution of 450 lines resulting from double-speed noninterlaced scanning for the field-line motion adaptive scanning line interpolation, reduction of cross-color and dot crawl resulting from frame-line motion adaptive Y-C separation, enhanced vertical and horizontal edge compensation, and an S-digital noise wiper for a maximum 8dB improvement in the video signal-to-noise ratio. Added functions include still, 3-mode strobe action, high picture quality S output terminals, and an RGB multiple 21-pin connector with automatic normal and double scan switching. For high audio quality, surround compatibility is provided with the variable system 2-way sealed speakers.(author abst.)

12/3,AB/15 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14484478 PASCAL No.: 00-0146367
Interface circuit for high-accuracy signal processing of differential-capacitance transducers
MOCHIZUKI K; MASUDA T; WATANABE K
Numazu Coll of Technology, Numazu, Japan
Journal: IEEE Transactions on Instrumentation and Measurement, 1998, 47 (4) 823-827
Language: English
An interface circuitry for high-accuracy signal processing of differential-capacitance transducers is developed. The architecture is based on the idea that the ratio of one of the transducer capacitances to its total capacitance represents the offset binary equivalent of the physical quantity under measurement. An opamp-based capacitance-to-voltage converter is commonly used for capacitance detection, and an analog-to-digital (A/D) converter is used for the ratiometric operation. Analyses show that the interface can detect the capacitance change as small as 0.01% of the total capacitance. Experimental results are also given to confirm the analyses.

12/3,AB/16 (Item 2 from file: 144)

12/20/2002

DIALOG(R)File 144:Pascal
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14119373 PASCAL No.: 99-0315190
Small-scaled InGaP/GaAs HBT's with WSi/Ti base electrode and buried SiO2
OKA T; HIRATA K; OUCHI K; UCHIYAMA H; **MOCHIZUKI K**; NAKAMURA T
Hitachi, Ltd, Tokyo, Japan
Journal: IEEE Transactions on Electron Devices, 1998, 45 (11) 2276-2282
Language: English
This paper describes the fabrication and characteristics of small-scaled InGaP/GaAs HBT's with high-speed as well as low-current operation. To reduce both the emitter size SE and the base-collector capacitance CBC simultaneously, the HBT's are fabricated by using WSi/Ti as the base electrode and by burying SiO2 in the extrinsic base-collector region under the base electrode. WSi/Ti simplifies and facilitates processing to fabricate a small base electrode, and makes it possible to reduce the width of the base contact to less than 0.4 mu m without the large increase in the base resistance. The DC current gain of 20 is obtained for an HBT with SE of 0.3x1.6 mu m2 due to the suppression of emitter size effect by using InGaP as the emitter material. An HBT with SE of 0.6x4.6 mu m2 exhibited fT of 138 GHz and fmax of 275 GHz at **IC** of 4 mA; and an HBT with SE of 0.3x1.6 mu m2 exhibited fT of 96 GHz and fmax of 197 GHz at **IC** of 1 mA. These results indicate the great potential of these HBT's for high-speed and low-power circuit applications.

12/3,AB/17 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal
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13140678 PASCAL No.: 97-0399926
Molecular beam deposition of n-type polycrystalline In SUB 0 SUB . SUB 6 Ga SUB 0 SUB . SUB 4 As for high resistances in heterojunction bipolar transistor **integrated circuits**
MOCHIZUKI K; OKA T; NAKAMURA T
Hitachi Ltd, Tokyo, Japan
Journal: Electronics Letters, 1997, 33 (13) 1181-1181
Language: English
100 nm thick n-type polycrystalline In SUB 0 SUB . SUB 6 Ga SUB 0 SUB . SUB 4 As layers have been grown on SiO SUB 2 by molecular beam epitaxy and their electrical properties have been investigated using Au/Pt/Ti as non-alloyed ohmic metals. A moderate sheet resistance of 4.7x10 SUP 2 &OHgr;/ square was obtained, together with a low specific contact resistance of 8x10 SUP - SUP 8 &OHgr;cm SUP 2 . This material should be useful for attaining high resistances in heterojunction bipolar transistor **integrated circuits**.

12/3,AB/18 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2002 INIST/CNRS. All rts. reserv.

07847438 PASCAL No.: 87-0327196
(Application of high temperature properties test results to blast furnace operation analysis and quality design of sinter)
MOCHIZUKI K; MURAI T; KAWAGUCHI Y; IWANAGA Y
Journal: Tetsu To Hagane, 1986-10, 72 (14) 1855-1861
Language: Japanese
Bericht ueber Aufheiz-Reduktionsversuche unter Last zur Untersuchung der Hochtemperatureigenschaften von verschiedenen in der Sinterpfanne hergestellten Sintersorten. Ableitung von Kriterien fuer **die**

Beurteilung der Sinterqualitaet anhand der Ergebnisse fuer Kaltfestigkeit und Reduktionsfestigkeit bei niedrigen Temperaturen. Aussagen ueber eine enge Beziehung zwischen Hochtemperatur-Sintereigenschaften und Hochofenleistung. Darstellung der Einfluesse der TI- und RI-Werte des Sinters auf den Brennstoffverbrauch des Hochofens. Eroerterung zur Einstellung der Sinterqualitaet fuer den Hochofenbetrieb. Hinweise auf **die** einzuschlagende Richtung der Untersuchungen zur weiteren Verbesserung der Sinterqualitaet.

12/3,AB/19 (Item 5 from file: 144)
DIALOG(R)File 144:Pascal

05971607 PASCAL No.: 85-0233089
Effect of the stoichiometry control on the photoelectrical properties of ZnS SUB x Se SUB 1 SUB - SUB x
MOCHIZUKI K; SUZUKI K
Tohoku Univ. Dept. of Materials Science, Sendai, Japan
Journal: Phys. status solidi (a), Appl. res., 1984-09, 85 (1) 249-256
Language: English
Es wird der Einfluss einer Stoechiometrieabweichung y von Zn SUB 1 SUB + SUB y (S SUB 0 SUB , SUB 2 SUB 5 Se SUB 0 SUB , SUB 7 SUB 5)-Einkristallen auf **die** photoelektrischen Eigenschaften untersucht. **Die** Stoechiometrie wird ueber den Wachstumsprozess aus der Dampfphase gesteuert, indem **die** Summe der Chalkogenpartialdruecke reguliert und das Verhaeltnis der Partialdruecke bei jeder Dampfphasenzuechtung konstant gehalten wird. Mit wachsender Partialdrucksumme nimmt **die** Emissionsintensitaet der breiten Bande, **die** bei 485,5nm (A-Maximum) beobachtet wird, zu, jedoch nehmen **die** Intensitaeten der Bandkantenemissionen und das Maximum der freien Exzitonen ab. **Die** elektrische Dunkelleitfaehigkeit bei Zimmertemperatur nimmt zu. **Die** Ergebnisse lassen sich durch das Anwachsen von Eigendefekten erklaeren.

12/3,AB/20 (Item 6 from file: 144)
DIALOG(R)File 144:Pascal

05289293 PASCAL No.: 83-0558634
lang. jap
(Mise au point d'une turbine pour le recyclage de l'energie et l'augmentation de la pression du gueulard)
(Development of blast furnace top pressure recovery turbine and dry gas cleaning system)
ASAI T; **MOCHIZUKI K**; TAKAWA T; KURASHIHE M; TANIDA K
Journal: Sumitomo kinzoku, 1982-10, 34 (3) 512-519
Language: Japanese
Vue d'ensemble des systemes developpes jusqu'a present pour l'utilisation du gaz du gueulard afin d'assurer simultanement un recyclage de l'energie et une augmentation de la pression dans le gueulard des hauts-fourneaux. Description d'une turbine axiale moderne dans la conduite d'evacuation d'un epurateur a voie humide. Perfectionement d'une turbine de recyclage, actionnee a sec, en utilisant des poches a filtre. Rapport sur les experiences faites jusqu'a present dans les usines siderurgiques de Kokura Ueberblick ueber bisher entwickelte Systeme fuer **die** Ausnutzung des Gichtgases zur gleichzeitigen Energiegewinnung und Druckerhoehung in der Gicht von Hochoefen. Beschreibung einer neuentwickelten axialen Turbine im Abstrom eines Nassgaswaeschers. Weiterentwicklung einer trockengehenden Rueckgewinnungsturbine unter Verwendung von Filtersaecken. Bericht ueber bisherige Erfahrungen in den Kokura-Huettenwerken.(H1)

12/20/2002

12/3,AB/21 (Item 7 from file: 144)
DIALOG(R)File 144:Pascal

05224393 PASCAL No.: 83-0491762
lang. jap
(Mise au point d'un systeme d'epuration en voie seche du gaz de gueulard d'un haut fourneau)
(Development of blast furnace gas dry cleaning system)
ASAI T; **MOCHIZUKI K**; YOKOI T; FUJIWARA T; ONO Y; TAKAWA T
Sumitomo Metal Industries Ltd., Osaka, Japan
Journal: Tetsu To Hagane, 1982-11, 68 (15) 2101-2107
Language: Japanese
Rapport concernant la turbine de detente axiale du gaz de gueulard du haut fourneau no 2 des usines Kokura de la societe Sumitomo Metal Ind. Ltd, et le systeme d'epuration sur filtre en voie seche du gaz de gueulard. Conseils pour la realisation du passage de la marche en voie humide en marche en voie seche
Bericht ueber **die** axiale Gichtgas-Entspannungsturbine am Hochofen Nr. 2 der Kokura-Werke von Sumitomo Metal Ind. Ltd. und das Trockenfilter-Gichtgasreinigungssystem. Aussagen ueber **die** Bewaehrung des Umbaus von nassen auf trockenen Betrieb.(H1)

16/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6789470 INSPEC Abstract Number: B2001-01-2830C-020
Title: Broadband measurement of the conductivity and the permittivity of semiconducting materials in high voltage XLPE cables
Author(s): Heinrich, R.; Bonisch, S.; Pommerenke, D.; Jobava, R.; Kalkner, W.
Author Affiliation: Tech. Univ. Berlin, Germany
Conference Title: Eighth International Conference on Dielectric Materials, Measurements and Applications (Conf. Publ. No.473) p.212-17
Publisher: IEE, London, UK
Publication Date: 2000 Country of Publication: UK xiv+522 pp.
ISBN: 0 85296 730 6 Material Identity Number: XX-2000-02736
Conference Title: Eighth International Conference on Dielectric Materials, Measurements and Applications
Conference Sponsor: IEE
Conference Date: 17-21 Sept. 2000 Conference Location: Edinburgh, UK
Language: English
Abstract: Because of several technical and economical advantages XLPE (cross-linked polyethylene)-insulated power cable systems are increasingly used in the high voltage (HV) and extremely high voltage (EHV) range. High voltage XLPE-insulated cables consist of a copper or aluminium conductor (inner conductor), a semiconducting layer extruded over the inner conductor, an XLPE-insulation, an outer semiconducting **layer**, a metallic **wire** screen or aluminum sheath and an outer polyethylene sheath. The extruded semiconducting layers provide a well bonded and smooth interface between the conductors and the dielectric, avoiding electric field strength enhancements, which would **lead** to partial discharge and a premature breakdown. However, the XLPE-insulation is very sensitive to partial discharges (PD). To ensure the reliability of the whole cable system, sensitive laboratory PD tests before installation and on-site verification are required. One common method to detect PD is the measurement of the radiated fields of the PD with sensitive field sensors. These sensors couple PD signals through the outer semiconducting layer and therefore the properties of the semiconducting layer have a significant influence on the coupling mechanisms. Knowing the conductivity and permittivity and their dependence on frequency and temperature is important to optimise PD field sensors. Those sensors are usually placed above the outer semicon layer close to or within cable joints. This paper presents a measurement set-up to determine the frequency dependent conductivity and permittivity of small samples taken from the outer semicon layer of different medium and high voltage cables. The measurement set-up can handle extremely high, frequency dependent dielectric constants, which are typical for semiconducting materials (carbon black filled polymers). Besides, the temperature of the sample can be adjusted from 10 degrees C to 85 degrees C to study the temperature dependence of the properties of the semicon sample.
Subfile: B

16/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6728905 INSPEC Abstract Number: B2000-11-2550F-073
Title: Pattern metallization on diamond thick film substrate
Author(s): Jiayu Wang; Hongyu Chen; Yizhen Bai; Xianyi Lu; Zengsun Jin

Author Affiliation: State Key Lab. of Superhard Mater., Jilin Univ., Changchun, China
Journal: Diamond and Related Materials Conference Title: Diam. Relat. Mater. (Switzerland) vol.9, no.9-10 p.1632-5
Publisher: Elsevier,
Publication Date: Sept.-Oct. 2000 Country of Publication: Switzerland
CODEN: DRMTE3 ISSN: 0925-9635
SICI: 0925-9635(200009/10)9:9/10L.1632:PMDT;1-0
Material Identity Number: A464-2000-006
U.S. Copyright Clearance Center Code: 0925-9635/2000/$20.00
Conference Title: IUMRS-ICAM'99 Symposium E: Diamond and Related Materials. 5th International Conference on Advanced Materials
Conference Date: 13-18 June 1999 Conference Location: Beijing, China
Language: English
Abstract: Diamond thick film with high thermal **conductivity** and high **electrical** resistivity has been synthesized with DC-hot cathode PCVD and EA-CVD methods. After being cut, polished and cleaned, diamond thick film was used as electronic packaging material. Pattern metallization on diamond thick film substrates was obtained using a thick-film-writing process. Transition metal ink was directly written on the diamond substrate as base ink. Then gold ink was printed on the transition metal ink. After pre-firing in the atmosphere at 450 degrees C for 10 min, the substrate was fired in a vacuum (1.33 Pa) at 850 degrees C for 30 min. Minimal or no gold blistering was observed from the fired diamond substrate, and the gold layer had not peeled after several heat impacts (25~450 degrees C). The result indicates that the fired metallization pattern has good adhesion to the diamond substrate. The chips were welded easily to the substrate and further electrically connected to the ground, power and signal **layers**, respectively, by **wire** bonding. The surface of the metallized substrate was characterized by scanning electron microscopy (SEM) and the carbide layer was analyzed by X-ray diffraction (XRD).
Subfile: B

16/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6052006 INSPEC Abstract Number: A9822-8245-011, B9811-2230-006
Title: Wire bonding over insulating substrates by electropolymerization of polypyrrole using a scanning micro-needle
Author(s): Shiratori, S.S.; Mori, S.; Ikezaki, K.
Author Affiliation: Dept. of Appl. Phys. & Physico-Inf., Keio Univ., Yokohama, Japan
Journal: Sensors and Actuators B (Chemical) Conference Title: Sens. Actuators B, Chem. (Switzerland) vol.B49, no.1-2 p.30-3
Publisher: Elsevier,
Publication Date: 25 June 1998 Country of Publication: Switzerland
CODEN: SABCEB ISSN: 0925-4005
SICI: 0925-4005(19980625)B49:1/2L.30:WBOI;1-9
Material Identity Number: N867-98010
U.S. Copyright Clearance Center Code: 0925-4005/98/$19.00
Conference Title: 9th International Solid State Sensors and Actuators Conference (Transducers '97)
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 16-19 June 1997 Conference Location: Chicago, IL, USA
Language: English
Abstract: **Electrically conducting** wires 10-200 mu m in diameter were controllably formed over electrically insulating substrates by electropolymerization of a conducting polymer using a scanning

micro-needle. The conductivity of the wire was estimated from the I-V characteristics to be about 0.5-200 S cm/sup -1/ which is not inferior to the reported conductivity of an electrochemically polymerized polypyrrole (PPy) **film**. **Wires** were formed like bridges between two conducting electrodes over glass substrates. This technique can be used for wire bonding of elements or electrodes.
Subfile: A B

16/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03589271 INSPEC Abstract Number: B90020486
Title: Thin-**film wiring** substrate for high density packaging with thin ceramic insulating layer
Author(s): Yamanaka, S.; Maeda, T.; Takikawa, T.; Ihara, T.; Igarashi, T.
Author Affiliation: Itami Res. Labs., Sumitomo Electric Ind. Ltd., Hyogo, Japan
Conference Title: Proceedings of the 5th International Microelectronics Conference p.330-7
Publisher: Int. Soc. Hybrid Microelectron, Tokyo, Japan
Publication Date: 1988 Country of Publication: Japan x+566 pp.
Conference Sponsor: ISHM
Conference Date: 25-27 May 1988 Conference Location: Tokyo, Japan
Language: English
Abstract: A new type wiring substrate for high density packaging has been developed based on thin-film technologies. As the demand for greater compactness, higher speed and improved performance in electronic devices increases, the demand for assembling materials and technologies needed to realize improved integration, speeds and performance has also increased. This new substrate has a multilayer construction in which alumina (Al/sub 2/O/sub 3/) thin-film insulating layers and aluminium (Al) thin-**film wiring** lines are **layered** on a metal plate. It suppresses crosstalk noise while permitting high density mounting of high speed LSI devices. These thin-film layers are formed by using a method based on radio-frequency ion plating evaporation. At the alumina thin-film layer where thickness is 3.5 mu m, the breakdown voltage is 400V (1MV/cm) or greater. Aluminium thin-film layer strongly adheres to the insulting layer; it has good wire bondability and good **electrical conductivity**. Since thin-film layers can be accurately applied, they can accommodate high density circuits on a **lead** frame, realizing a **lead** frame type multi-chip module.
Subfile: B

16/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

02870919 INSPEC Abstract Number: A87058792
Title: Temperature dependence of electrical resistivity for gold and **lead**
Author(s): Nishi, Y.; Igarashi, A.; Mikagi, K.
Author Affiliation: Dept. of Mater. Sci., Tokai Univ., Hiratsuka, Japan
Journal: Journal of Materials Science Letters vol.6, no.1 p.87-8
Publication Date: Jan. 1987 Country of Publication: UK
CODEN: JMSLD5 ISSN: 0261-8028
U.S. Copyright Clearance Center Code: 0261-8028/87/$03.00+.12
Language: English

Abstract: Using **wire**, **film** and sheet specimens, the authors have found that R(T), which is the temperature-dependent term arising from the dynamic deviations from crystal perfection, is related to T for T>T/sub D//2, T/sup 2/ for T/sub D//6<T<T/sub D//2 and T/sup 4/ for T/sub D//12<T<T/sub D//6 where T/sub D/ is Debye temperature. It has also been found that (d log R(t)/d log T) decreased discontinuously with temperature and therefore three individual models have to be considered for the three stages.
Subfile: A

16/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02675679 INSPEC Abstract Number: A86070925
Title: Role of quantum coherence in series resistors
Author(s): Buttiker, M.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: Physical Review B (Condensed Matter) vol.33, no.5 p.3020-6
Publication Date: 1 March 1986 Country of Publication: USA
CODEN: PRBMDO ISSN: 0163-1829
Language: English
Abstract: Landauer's approach which yields the resistance of an obstacle in an otherwise perfect **wire** due to **elastic** scattering at the obstacle is augmented by including localized inelastic scatterers within the sample. The inelastic scatterers invoked consist of an electron reservoir coupled via a **lead** to the wire. The key advantage of this method is that the effect of inelastic scattering can be studied by solving an elastic scattering problem. The author investigates the resistance of a series of two (or more) obstacles and study the transition from completely coherent transmission through the sample to completely incoherent transmission. For a sample with a small transmission probability, increasing inelastic scattering decreases the resistance. At an intermediate value of inelastic scattering, the resistance reaches a minimum to increase again when inelastic scattering processes start to dominate the resistance.
Subfile: A

16/3,AB/7 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

2181226 NTIS Accession Number: N20000083956/XAB
Thin and Thick Films Materials Based Interconnection Technology for 500 C Operation
Chen, L. Y. ; Hunter, G. W. ; Neudeck, P. G.
National Aeronautics and Space Administration, Cleveland, OH. NASA John H. Glenn Research Center at Lewis Field.
Corp. Source Codes: 115801001; ZT002737
Report No.: NAS 1.15:209940; NASA/TM-2000-209940,E-12188
Aug 2000 10p
Languages: English
Journal Announcement: USGRDR0026; STAR3802
Presented at First International Conference on Microelectronics and Interfaces 1st Santa Clara, CA 7-11 Feb. 2000. American Vacuum Society, New York, NY.
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email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Precious metal based thick-film material was used for printed wires, wire bond pads, test **lead** -attach, and conductive die-attach for high temperature (up to 500 C and beyond) chip level packaging. A SiC Shottky diode with a thin-film coated backside was attached to a ceramic substrate using precious metal based thick-film material as the **electrically conductive** bonding layer. After a 500-hour soak test in atmospheric oxygen, these basic interconnection elements, including attached test diode survived both electrically and mechanically. The electrical resistance of these interconnections (including thick-**film** printed **wire**/pad, bonded wire, and test **lead** attach) were low and stable at both room and elevated temperatures. The electrical resistance of the die-attach interface estimated by I-V characterization of the attached diode, during and after high temperature heat treatment, remained desirably low over the course of a 500-hour anneal. Further durability testing of this high temperature interconnection technology is also discussed.

16/3,AB/8 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

2047965 NTIS Accession Number: ASTM-B 784-94/XAB
Modified Concentric-Lay-Stranded Copper Conductors for Use in Insulated Electrical Cables. (ASTM Standard)
American Society for Testing and Materials, West Conshohocken, PA.
Corp. Source Codes: 113500000
cOct 94 5p
Languages: English
Journal Announcement: GRAI9808
This specification is under the jurisdiction of ASTM Committee B-1 on Electrical Conductors and is the direct responsibility of Subcommittee B01.04 on Conductors of Copper and Copper Alloys. Current edition approved Aug. 15, 1994. Published October 1994. Originally published as B784-88. Last previous edition B784-93 .
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NTIS Prices: PC$27.00

16/3,AB/9 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

2020353 NTIS Accession Number: ASTM-B 8-95/XAB
Concentric-Lay-Stranded Copper Conductors, Hard, Medium-Hard, or Soft. (ASTM Standard)
American Society for Testing and Materials, West Conshohocken, PA.
Corp. Source Codes: 113500000
cOct 95 7p
Languages: English
Journal Announcement: GRAI9723
DoD adopted. This specification is under the jurisdiction of ASTM Committee B-1 on Electrical Conductors and is the direct responsibility of

Subcommittee B01.04 on Conductors of Copper and Copper Alloys. Current edition approved Aug. 15, 1995. Published October 1995. Originally published as B8-15T. Last previous edition B8-93.
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NTIS Prices: PC$27.00

16/3,AB/10 (Item 4 from file: 6)
DIALOG(R)File 6:NTIS

2020128 NTIS Accession Number: ASTM-B 189-95/XAB
Lead-Coated and **Lead**-Alloy-**Coated** Soft Copper **Wire** for Electrical Purposes. (ASTM Standard)
American Society for Testing and Materials, West Conshohocken, PA.
Corp. Source Codes: 113500000
cSep 95 6p
Languages: English
Journal Announcement: GRAI9723
DoD adopted. This specification is under the jurisdiction of ASTM Committee B-1 on Electrical Conductors and is the direct responsibility of Subcommittee B01.04 on Conductors of Copper and Copper Alloys. Current edition approved July 15, 1995. Published September 1995. Originally published as B189-44T. Last previous edition B189-90.
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NTIS Prices: PC$27.00

16/3,AB/11 (Item 5 from file: 6)
DIALOG(R)File 6:NTIS

2020121 NTIS Accession Number: ASTM-B 174-95/XAB
Bunch-Stranded Copper **Conductors** for **Electrical Conductors**. (ASTM Standard)
American Society for Testing and Materials, West Conshohocken, PA.
Corp. Source Codes: 113500000
cSep 95 4p
Languages: English
Journal Announcement: GRAI9723
DoD adopted. This specification is under the jurisdiction of ASTM Committee B-1 on Electrical Conductors and is the direct responsibility of Subcommittee B01.04 on Conductors of Copper and Copper Alloys. Current edition approved July 15, 1995. Published September 1995. Originally published as B158-41T. Last previous edition B174-90.
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NTIS Prices: PC$22.50

16/3,AB/12 (Item 6 from file: 6)
DIALOG(R)File 6:NTIS

2020120 NTIS Accession Number: ASTM-B 173-95/XAB
Rope-Lay-Stranded Copper Conductors Having Concentric-Stranded Members, for **Electrical Conductors**. (ASTM Standard)
American Society for Testing and Materials, West Conshohocken, PA.
Corp. Source Codes: 113500000
cSep 95 5p
Languages: English
Journal Announcement: GRAI9723
DoD adopted. This specification is under the jurisdiction of ASTM Committee B-1 on Electrical Conductors and is the direct responsibility of Subcommittee B01.04 on Conductors of Copper and Copper Alloys. Current edition approved July 15, 1995. Published September 1995. Originally issued 1942 to replace portions of B158-41T. Last previous edition B173-90.
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NTIS Prices: PC$27.00

16/3,AB/13 (Item 7 from file: 6)
DIALOG(R)File 6:NTIS

2020119 NTIS Accession Number: ASTM-B 172-95/XAB
Rope-Lay-Stranded Copper Conductors Having Bunch-Stranded Members, for **Electrical Conductors**. (ASTM Standard)
American Society for Testing and Materials, West Conshohocken, PA.
Corp. Source Codes: 113500000
cSep 95 4p
Languages: English
Journal Announcement: GRAI9723
DoD adopted. This specification is under the jurisdiction of ASTM Committee B-1 on Electrical Conductors and is the direct responsibility of Subcommittee B01.04 on Conductors of Copper and Copper Alloys. Current edition effective July 15, 1995. Published September 1995. Originally issued 1942 to replace portions of B158-41 T. Last previous edition B172-90.
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NTIS Prices: PC$22.50

16/3,AB/14 (Item 8 from file: 6)
DIALOG(R)File 6:NTIS

1867091 NTIS Accession Number: DE95003718
HTS current **lead** using a composite heat pipe
Daugherty, M. A. ; Prenger, F. C. ; Hill, D. D. ; Daney, D. E. ; Woloshun, K. A.
Los Alamos National Lab., NM.
Corp. Source Codes: 072735000; 9512470
Sponsor: Department of Energy, Washington, DC.
Report No.: LA-UR-94-3725
1995 5p
Languages: English
Journal Announcement: GRAI9511; ERA9519
Applied superconductivity conference, Boston, MA (United States), 16-21 Oct 1994. Sponsored by Department of Energy, Washington, DC.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A01/MF A01
This paper discusses the design and fabrication of HTS current leads being built by Los Alamos to supply power to a demonstration HTS coil which will operate in a vacuum cooled by a cryocooler. Because vapor cooling is not an option for this application the leads must be entirely conductively cooled. In the design of HTS current leads for this type of application, it is desirable to intercept part of the heat load at an intermediate temperature. This thermal intercept or connection must be electrically insulating but thermally conductive, two mutually exclusive properties of most candidate solid materials. To achieve this end we incorporate a composite nitrogen heat pipe, constructed of conducting and non-conducting materials, to provide efficient thermal communication and simultaneously, electrical isolation between the **lead** and the intermediate temperature heat sink. Another important feature of the current **lead** design is the use of high Jc thick film superconductors deposited on a non-conducting substrate to reduce the conductive heat leak through the lower portion of the **lead**. Two flexible **electrical conductors** are incorporated to accommodate handling, assembly and the dissimilar expansion coefficients of the various materials.

16/3,AB/15 (Item 9 from file: 6)
DIALOG(R)File 6:NTIS

1075548 NTIS Accession Number: AD-A134 193/2
Development of the Mk-112 Detonator
(Final rept. Sep 80-Sep 82)
Baudler, B. A. ; Simpson, B.
Naval Surface Weapons Center, Silver Spring, MD.
Corp. Source Codes: 043878000; 411563
Sponsor: Shared Bibliographic Input.
Report No.: NSWC/TR-82-482; SBI-AD-F500 167
1 Dec 82 35p
Languages: English
Journal Announcement: GRAI8404
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A03/MF A01
A new detonator, the Mk-112, has been developed and evaluated as a possible replacement for the Mk 57 mod 1 detonator. Its use may be necessary in applications where **lead** wires are desired in place of contact pins. The Mk-112 has also been designed to be protected from hazards of electrostatic discharge by the application of a conductive coating, Electrodag R plus 501, and a protective varnish to the back of each detonator plug. By doing so, a low resistance electrical contact will be formed between the **lead** wires and detonator case. These coatings can be applied at a minimal cost and were able to withstand all environmental and mechanical conditions required by MIL-I-23659 for EED design.

16/3,AB/16 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03571524
E.I. Monthly No: EIM9303-011637
Title: Three-dimensionally interconnected metal spring network in a silicone matrix as a resilient and **electrically conducting** composite material.
Author: Zhu, Mingguang; Chung, D. D. L.
Corporate Source: State Univ of New York at Buffalo, Buffalo, NY, USA
Conference Title: 6th International SAMPE Electronics Conference
Conference Location: Baltimore, MD, USA Conference Date: 19920622
E.I. Conference No.: 17353
Source: International SAMPE Electronics Conference v 6 1992. p 770-781
Publication Year: 1992
CODEN: ISECE8 ISBN: 0-938994-65-4
Language: English
Abstract: Isotropic, highly resilient and **electrically conducting** composites in the form of silicone-matrix copper-spring three-dimensional network composites were developed for use as electrical and thermal contact materials. The springs were made from 63 mu m diameter copper **wires** and were **coated** and interconnected by Sn-Pb solder. In the composites, the springs were long, bent, intersecting and interconnected to one another to form a three-dimensional network. Composites are fabricated by infiltration of a silicone resin into a preform of springs. A volume resistivity of 5 multiplied by 10** minus **4 Omega .cm, a contact resistivity with copper of 0.016 Omega .cm**2 at greater than equivalent to 0.03 MPa, and a permanent set of 0.6% after compression at 0.4 MPa were achieved in a silicone-matrix composite containing 3.1 vol.% Cu springs and 2.9 vol.% solder (i.e., 6.0 vol.% total filler); the volume resistivity was not affected by heating in air at 130-150 degree C for 7 days, nor by immersion in water for 7 days. The volume resistivity values of composites containing from 4.17 to 6.00 vol.% total filler were equal to 3 times the corresponding calculated values for composites containing unidirectional and continuous fibers, indicating that the filler was indeed a continuous three-dimensional network. (Author abstract) 10 Refs.

16/3,AB/17 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05268979 JICST ACCESSION NUMBER: 02A0787225 FILE SEGMENT: JICST-E
Development of High Performance **Coated Wire** Electrodes for High-speed Cutting and Accurate Machining.

KURODA HIROMITSU (1); AOYAMA SEIGI (1); KIMURA TAKAMITSU (2)
(1) Hitachi Cable, Ltd., JPN; (2) Hitachi Cable, Ltd.
Do to Dogokin(Journal of Japan Research Institute for Advanced Copper-Base Materials and Technologies), 2002, VOL.41, PAGE.237-240, FIG.8, TBL.2, REF.5
JOURNAL NUMBER: S0603ABO ISSN NO: 1347-7234
UNIVERSAL DECIMAL CLASSIFICATION: 621.9.047/.048 669-419
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Electric discharge machining(EDM) is an important technology for precision manufacturing of such items as metal molds for IC **lead** frames and electronic parts. Wire electric discharge machining demands high-speed cutting and high-precision machining to realize productivity and improved accuracy of metal molds. We considered two types of **coated wire** electrodes. Both consist of a thin copper zinc alloy layer and core material and one is a copper zinc alloy coated with a brass layer while the other is a Cu-Sn-In alloy with high heat resistance and high **electrical conductivity**. We studied use of a coating layer with a high concentration of zinc and then developed the HIR electrode for high-speed and accurate cutting and the HIS electrode for super-high-speed cutting. (author abst.)

16/3,AB/18 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01179512 JICST ACCESSION NUMBER: 90A0847250 FILE SEGMENT: JICST-E
A conductance study of macrocyclic schiff base metal(II) complexes in methanol.
LIU J (1); MASUDA Y (1); SEKIDO E (1)
(1) Kobe Univ., Kobe
Bull Chem Soc Jpn, 1990, VOL.63,NO.9, PAGE.2516-2520, FIG.3, TBL.5, REF.20
JOURNAL NUMBER: G0450AAJ ISSN NO: 0009-2673 CODEN: BCSJA
UNIVERSAL DECIMAL CLASSIFICATION: 544.142.3.032.1 544.142.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The first ionic association constants between five macrocyclic schiff base metal(II) complexes (cation and perchlorate or thiocyanate anion) were determined by conductometric measurements in methanol at 25.DEG.C. by using a modified Onsager limiting equation, according to Fuoss and Edelson method. The limiting equivalent conductivities of the chelate cations of these complexes were calculated. These results were used to evaluate the performance of **coated-wire** perchlorate ion-selective electrodes (PCWE) based on these complexes. (author abst.)

16/3,AB/19 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15494448 PASCAL No.: 02-0189813
Destruction of the global phase coherence in ultrathin, doubly connected superconducting cylinders
LIU Y; ZADOROZHNY Yu; ROSARIO M M; ROCK B Y; CARRIGAN P T; WANG H
Department of Physics, The Pennsylvania State University, University

Park, PA 16802, United States
Journal: Science : (Washington, D.C.), 2001, 294 (5550) 2332-2334
Language: English
In doubly connected superconductors, such as hollow cylinders, the fluxoid is known to be quantized, allowing the superfluid velocity to be controlled by an applied magnetic flux and the sample size. The sample-size-induced increase in superfluid velocity has been predicted to **lead** to the destruction of superconductivity around half-integer flux quanta. We report transport measurements in ultrathin Al and Au SUB 0 SUB . SUB 7 In SUB 0 SUB . SUB 3 cylinders verifying the presence of this destructive regime characterized by the loss of the global phase coherence and reveal a phase diagram featuring disconnected phase coherent regions, as opposed to the single region seen in larger superconducting cylinders studied previously.

16/3,AB/20 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

13710631 PASCAL No.: 98-0401606
Electrical properties and corrosion of Bi-2223 **coatings** on silver **wires** directly synthetized from a Bi-2223 precursor or from a Bi-2223/Bi-2212 mixture
LAMINE C; BEN AZOUZ F; BADECHE T; MONNEREAU O; BEN SALEM M; BOULESTEIX C
MUSSO J, ed; GAVARRI J R, ed
MATOP, URA 1530, Case 151, Faculte des Sciences de Saint Jerome, 13397 Marseille, France; Laboratoire de Physique des Materiaux, Faculte des Sciences de Bizerte, Tunisia; LPCM, Universite de Provence, 3 place Victor Hugo, 13331 Marseille, France
Laboratoire Materiaux Multiphases et Interfaces (MMI), Faculte des Sciences et Techniques, Universite de Toulon-Var, BP. 132, 83957 La Garde, France
CCAS1 Colloque sur les composites actifs supraconducteurs, 1 (Toulon-La Garde FRA) 1996-09-11
Journal: Journal de physique. IV, 1998, 8 (1) Pr1.51-Pr1.55
Language: English
Superconducting wires are prepared by coating of a silver substrate, by sintering of a slurry deposited onto the metal core and containing a grinded (Pb doped) Bi-2223 ceramic, a grinded Bi-2223/Bi-2212 mixed ceramic or a grinded mixture of the Bi-2223 precursors, and of 20% PbO in excess. The resistance-versus-temperature R(T) curves obtained for a 6 days sintering at 835 Degree C presented only one drop, with Tc0 = 108K (107K when the slurry is a mixture of the Bi-2223 precursors). When the coating is obtained from a grinded Bi-2223/Bi-2212 mixed ceramic the R(T) curves are better (higher Tc and narrower DELTA Tc) than the R(T) curves obtained with the ceramic used for preparing the wires, for which Tc0 = 34K. The role of PbO in excess is discussed.These coatings hold rather well against corrosion by waper vapor at 90 Degree C and the Bi-2223 phase is less corroded than the Bi-2212 phase.

16/3,AB/21 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

10337556 PASCAL No.: 92-0541016

12/20/2002

A three-dimensionally interconnected metal-spring network in a silicone matrix as a resilient and **electrically conducting** composite material

MINGGUANG ZHU; CHUNG D D L

State univ. New York at Buffalo, composite materials res. lab., Buffalo NY 14260, USA

Journal: Composites, 1992, 23 (5) 355-363

Language: English

Isotropic, highly resilient and **electrically conducting** composites in the form of a copper-spring three-dimensional network embedded in a silicone matrix were developed for use as electrical and thermal contact materials. The springs were made from 63 mu m diameter copper **wires** and were **coated** and interconnected by Sn-Pb solder. The springs used were long coils, intersecting and interconnected to one another to form a three-dimensional network. Composites were fabricated by infiltration of a silicone resin into a preform of springs

16/3,AB/22 (Item 4 from file: 144)

DIALOG(R)File 144:Pascal

09545170 PASCAL No.: 91-0335598

Fabrication of Bi-Pb-Sr-Ca-Cu-O superconducting composite wires with copper core

GROZAV A D; KONOPKO L A; LEPORDA N I; ONU M I; PANAITOV G I

Moldavian acad. sci., inst. applied physics, Kishinev 277028, Union of Soviet Socialist Republics

Journal: Solid state communications, 1990, 76 (8) 1023-1026

Language: English

By passing a **flexible** copper **wire** through the molten Bi-Pb-Sr-Ca-Cu-O system at a high constant speed, long lengths of composite wires were prepared. Depending on the pulling speed and the temperature of the melt, a coating with different microstructure and thickness from less than ten to several tens of microns can be obtained. The short samples cut out of the composite wires thus obtained were annealed in air in a preheated furnace. After relatively short-time annealing at 800 Degree C, both resistivity and d.c. magnetization versus temperature measurements show indications of onset of superconductivity in the 110-115 K region; zero resistance was achieved in the range 65-70 K

12/20/2002

19/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7387851 INSPEC Abstract Number: B2002-10-7230-053, C2002-10-3240M-003
Title: Digital tactile sensing elements communicating through conductive skin layers
Author(s): Hakozaki, M.; Shinoda, H.
Author Affiliation: Graduate Sch. of Inf. Phys. & Comput., Tokyo Univ., Japan
Conference Title: Proceedings 2002 IEEE International Conference on Robotics and Automation (Cat. No.02CH37292) Part vol.4 p.3813-17 vol.4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA 4 vol.lxxiv+4353 pp.
ISBN: 0 7803 7272 7 Material Identity Number: XX-2002-01953
U.S. Copyright Clearance Center Code: 0-7803-7272-7/02/$17.00
Conference Title: Proceedings 2002 IEEE International Conference on Robotics and Automation
Conference Sponsor: IEEE Robotics & Autom. Soc
Conference Date: 11-15 May 2002 Conference Location: Washington, DC, USA
Language: English
Abstract: In this paper, we propose a tactile sensing element that communicates through two dimensional conductive skin **layers** without individual **wires** . Each tactile element has sensors and signal processors, and it broadcasts coded tactile signals through a couple of conductive layers. Since the conductive layers can be used for both the electrical power supply and the communication, simply sandwiching the **chips** between the layers completes **electrical connection** of tactile sensing **chips**. Since no metal wires exist, the skin is elastic and tough. High-resolution sensor skins can be easily fabricated in various shapes. In addition, because the tactile elements transmit the locally detected stress data with coded signals, we can obtain high-SN-ratio data from a very small sensing element put at a remote location. This paper describes the skin structure, the communication architecture, the structure of the sensing **chip**, and the results of basic experiments.
Subfile: B C

19/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6254944 INSPEC Abstract Number: B1999-07-0170J-008
Title: Evolution of engineering change and repair technology in high performance multichip modules at IBM
Author(s): Perfecto, E.D.; Ray, S.K.; Wassick, T.A.; Stoller, H.
Author Affiliation: IBM Microelectron., Hopewell Junction, NY, USA
Journal: IEEE Transactions on Advanced Packaging vol.22, no.2 p. 129-35
Publisher: IEEE,
Publication Date: May 1999 Country of Publication: USA
CODEN: ITAPFZ ISSN: 1521-3323
SICI: 1521-3323(199905)22:2L.129:EECR;1-3
Material Identity Number: H273-1999-002
U.S. Copyright Clearance Center Code: 1521-3323/99/$10.00

Language: English
Abstract: In multichip modules (MCMs), engineering changes (EC) are required for both repair of defective **chip** to **chip** connections within the module, as well as modification of **electrical connections** for module performance optimization. With the recent use of complementary metal-oxide-semiconductor (CMOS) **chips** in IBM's latest generation of mainframe machines, EC design has been modified to accommodate **chips** with a much higher number of signal I/Os. Using the previous design methodology of connecting each signal C4 to an EC pad, a large area of the top surface of the module would be required for EC features. This would force increased **chip**-to-**chip** wiring length and impact module performance. In addition, larger size MCMs would be required, driving up cost. The new EC approach utilizes top surface thin **film wiring** in the X and Y directions, which is not pre-connected to any signal C4 pads. The approach used to make desired EC connections is described. New processes were developed to make micro-connections to customize an EC connection, CMOS based MCMs have more than 5* the signal I/Os per **chip** compared to bipolar devices. As a result of the evolution in EC technology, CMOS **chip** based MCMs have been successfully designed, built, tested and debugged quickly. They are being used in IBM's latest generation mainframe machines.
Subfile: B

19/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6083450 INSPEC Abstract Number: B9812-2250-013
Title: Evolution of engineering change (EC) and repair technology in high performance multi-**chip** modules at IBM
Author(s): Perfecto, E.D.; Ray, S.; Wassick, T.A.; Stoller, H.
Author Affiliation: IBM Microelectron., Hopewell Junction, NY, USA
Conference Title: 1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206) p.916-21
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xxv+1476 pp.
ISBN: 0 7803 4526 6 Material Identity Number: XX98-01334
U.S. Copyright Clearance Center Code: 0 7803 4526 6/98/$10.00
Conference Title: 1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206)
Conference Sponsor: IEEE Components, Packaging & Manuf. Technol. Soc.; Electron. Ind. Assoc
Conference Date: 25-28 May 1998 Conference Location: Seattle, WA, USA
Language: English
Abstract: In Multi-**Chip** Modules (MCM), engineering changes (EC) are required for both repairs of defective **chip** to **chip** connections within the module, as well as to modify **electrical connections** for module performance optimization. In IBM's TCM technology, used in previous generation bipolar devices, 100% EC capability was designed in by connecting each signal I/O pad on the **chip** through a C4 solder connection on the module to a top surface EC pad. The EC pad is connected to an internal net via a delete strap. New connections can be made between **chips** on the MCM, by first laser deleting the internal nets, and bonding discrete EC wires, and routing these to desired locations on the top surface of the module. The main drawbacks of this design approach were threefold: EC pads took up valuable real estate around each **chip** site, the near end coupled noise among long lengths of discrete EC wires on the top surface of the module was prohibitive and the insulated discrete wires used to make EC connections required unique wire bond and routing

tools. With the recent use of CMOS **chips** in IBM's latest generation of mainframe machines, EC design has been modified to accommodate **chips** with much higher number of signal I/Os. Using the previous design methodology of connecting each signal C4 to an EC pad, a large area of the top surface of the module would be required for EC features. This would have forced increased **chip** to **chip** wiring length and impacted module performance. In addition, larger size MCMs would be required, driving up cost. The new EC approach utilizes top surface thin **film wiring** in the X and Y directions, which are not pre-connected to any signal C4 pads. The approach used to make desired EC connections is described. New processes were developed to make micro-connections to customize an EC connection. CMOS based MCMs have more than 5* the signal I/Os per **chip** compared to bipolar devices. As a result of the evolution in EC technology, CMOS **chip** based MCMs have been successfully designed, built, tested and debugged quickly. They are being used in IBM's latest generation mainframe machines.
Subfile: B

19/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6046773 INSPEC Abstract Number: B9811-2250-025
Title: Bare **chip** stacking structure for MCM production
Author(s): Kimura, T.; Okuda, O.; Ishikawa, H.; Suzuki, Y.; Hodges, C.R.; Kim, P.; Nakajima, K.
Author Affiliation: Sumitomo Metal Min. Co. Ltd., Tokyo, Japan
Conference Title: Proceedings. 1998 International Conference on Multichip Modules and High Density Packaging (Cat. No.98EX154) p.303-7
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xi+547 pp.
ISBN: 0 7803 4850 8 Material Identity Number: XX98-01189
U.S. Copyright Clearance Center Code: 0 7803 4850 8/98/$10.00
Conference Title: Proceedings 1998 International Conference on Multichip Modules and High Density Packaging
Conference Sponsor: IMAPS; IEEE; CPMT; MCM; EIA
Conference Date: 15-17 April 1998 Conference Location: Denver, CO, USA
Language: English
Abstract: In order to obtain higher density and lower cost multichip modules (MCM), we have developed a simply structured bare-**die** stacking assembly technology. It provides a simple structure with thick epoxy layer to fix upper layer bare **die** , rather than custom structures such as notched dies or additional electrodes at **die** edge in the conventional structures. The developed technology can use exactly the same dies as those for wire bonding interconnection without any additional processing. All **electrical connections** of the upper and lower dies are achieved by wire-bonding to the substrate independently. We have performed this stacking assembly by precise control of epoxy **layer** thickness and **wire** loop shapes. This new technology was applied to the production of MCMs, including twelve memory dies. The assembled MCM was almost twice as dense as an MCM without a stacked-**die** structure. The MCM were verified to functional correctly. The assembly yield of MCM with this structure was high enough for production. As our technology includes a repair method for failed dies, fully tested KGD (known good **die**) are not necessary.
Subfile: B

12/20/2002

19/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6040123 INSPEC Abstract Number: B9811-2250-016
Title: Fabrication and characterization of a high temperature superconducting multichip module
Author(s): Cooksey, J.W.; Brown, W.D.; Schaper, L.W.; Florence, R.G.; Scott, S.S.; Afonso, S.
Author Affiliation: Dept. of Electr. Eng., Arkansas Univ., Fayetteville, AR, USA
Conference Title: Proceedings of the Fourth Symposium on Low Temperature Electronics and High Temperature Superconductivity p.100-7
Editor(s): Claeys, C.L.; Raider, S.I.; Deen, M.J.; Brown, W.D.; Kirschman, R.K.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA ix+402 pp.
ISBN: 1 56677 129 3 Material Identity Number: XX98-01456
Conference Title: Proceedings of the Fourth Symposium on Low Temperature Electronics and High Temperature Superconductivity
Conference Sponsor: Electrochem. Soc
Conference Date: 4-11 May 1997 Conference Location: Montreal, Que., Canada
Language: English
Abstract: A process for fabricating high temperature superconducting (HTS) multichip module-deposited (MCM-D) substrates has been developed and tested. The module consists of two digital gallium arsenide bare **die** connected by YBa/sub 2/Cu/sub 3/O/sub 7- delta / (YBCO) HTS interconnects to form two ring oscillators on a 2.25 cm/sup 2/ MCM-D substrate. The interconnections consist of two **wiring layers** of YBCO separated by a 4-5 mu m silicon dioxide interlevel dielectric. The 50 mu m wide signal lines are routed between 150 mu m power and ground lines with 75 mu m spacings to form an interconnected mesh power system (IMPS). Connection between the two YBCO layers is accomplished with low contact resistance 40 mu m gold vias through the interlevel dielectric **layer**. Ultrasonic Al **wire** bonds serve as **electrical connections** to gold/YBCO bond pads on the MCM substrate.
Subfile: B

19/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5665080 INSPEC Abstract Number: B9709-2250-023
Title: Recent advances in high temperature superconductor multichip modules
Author(s): Cooksey, J.W.; Scott, S.S.; Brown, W.D.; Ang, S.S.; Florence, R.G.
Author Affiliation: Dept. of Electr. Eng., Arkansas Univ., Fayetteville, AR, USA
Conference Title: Proceedings. 1997 International Conference on Multichip Modules (Cat. No.97TH8258) p.115-20
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA x+379 pp.
ISBN: 0 7803 3787 5 Material Identity Number: XX97-00823
U.S. Copyright Clearance Center Code: 0 7803 3787 5/97/$5.00
Conference Title: Proceedings 1997 International Conference on Multichip Modules
Conference Sponsor: IEPS; ISHM; IEEE; EIA; SEMI; PCMCIA Assoc.; IPC

Conference Date: 2-4 April 1997 Conference Location: Denver, CO, USA
Language: English
Abstract: Two different techniques for fabricating high temperature superconducting (HTS) MCM-D substrates have been developed and tested. The first unit consists of two digital gallium arsenide bare **die** connected by YBa/sub 2/Cu/sub 3/O/sub 7- delta / (YBCO) HTS interconnects to form two ring oscillators on a 2.25 cm/sup 2/ MCM-D substrate. The interconnections consist of two **wiring layers** of YBCO separated by a 4-5 mu m silicon dioxide interlevel dielectric. The signal lines are routed between power and ground lines which form an interconnected mesh power system (IMPS) and, thereby, the module avoids the necessity of having two additional layers for power and ground planes. Connection between the two YBCO layers is accomplished with low contact resistance 40 mu m gold vias through the interlevel dielectric layer. The signal interconnects have 50 mu m linewidths and 75 mu m spacings. **Electrical connections** between the **die** and the MCM substrate and between the substrate and the PC board were made using ultrasonic Al wire bonds to low contact resistance gold/YBCO bondpads on the MCM substrate. The second module, known as the Flip-Mesh superconducting MCM; provides an alternative to the multilayer MCM-D substrate described above. It involves using flip **chip** bonding techniques to connect multiple single-layer substrates, thereby reducing the processing complexity of fabricating multiple layers. X-plane and Y-plane interconnects are fabricated on separate substrates and interconnected using solder bumps. The IMPS topology is also utilized in this structure so that power, ground, and signals can be fabricated on two planes. The initial Flip-Mesh design incorporates 100 mu m (4 mil) solder bump vias with similar spacings, which results in a low packing density for MCM-D technology, but a high density for I/O technology.
Subfile: B

19/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

4938806 INSPEC Abstract Number: B9506-2240-005
Title: Wire bonding: Present and future trends
Author(s): Chen, A.S.; Nguyen, L.T.; Burke, T.S.; Belani, J.G.
Author Affiliation: Nat. Semicond. Corp., Santa Clara, CA, USA
p.45-51
Publisher: IEEE, New York, NY, USA
Publication Date: 1993 Country of Publication: USA xii+504 pp.
ISBN: 0 7803 1424 7
U.S. Copyright Clearance Center Code: 0 7803 1424 7/93/$3.00
Conference Title: Proceedings of 15th IEEE/CHMT International Electronic Manufacturing Technology Symposium
Conference Sponsor: Electron. Ind. Assoc.; Components, Hybrids & Manuf. Technol. Soc
Conference Date: 4-6 Oct. 1993 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: Gold wire thermosonic bonding remains the primary means of **electrically connecting** the silicon **chip** to the outside world. To keep up with the increasing interconnect density required by the ever shrinking **die** and with the need for package compactness, both wire and wire bonder manufacturers have made many improvements in technology. If the miniaturization trend continues at the current rate, the physical and process limits will ultimately be reached. The other possible technologies such as gold wedge bonding, tape automated bonding (TAB), and flip-**chip** offer some potential attractive interconnection solutions.

These techniques also have their own inherent disadvantages. Until such drawbacks are resolved, the capabilities of thermosonic bonding will continue to be pushed as far as possible.
Subfile: B

19/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

04043855 INSPEC Abstract Number: B9201-6430H-014
Title: A subminiature CCD module using a new assembly technique
Author(s): Kondoh, Y.; Saito, M.
Author Affiliation: Res. & Dev. Center, Toshiba Corp., Kawasaki, Japan
Journal: IEICE Transactions vol.E74, no.8 p.2355-61
Publication Date: Aug. 1991 Country of Publication: Japan
CODEN: IEITEF ISSN: 0917-1673
Language: English
Abstract: A bare CCD **chip** is mounted directly on an optical glass substrate, and the outer circuit is connected to the surface of the glass substrate. This work needs two important assembly techniques. One is the COG bonding technique, and the other is the glass outer connecting technique. In the COG bonding technique, gold bumps are formed on aluminum pads of a CCD **chip** using the ball bonding method. A thick gold **film wiring** pattern and indium-alloy bumps are formed on the glass substrate. The CCD **chip** is pressed onto the glass substrate, and is heated. The CCD **chip** is **connected electrically** to the glass substrate. The glass outerconnecting technique is that of connecting an FPC (flexible printed circuit) to the glass substrate. The authors decided to use ACF (anisotropic conductive film) connection. The manufactured subminiature CCD module was small, one-fifth in volume, and light, one-tenth in weight, compared with conventional types.
Subfile: B

19/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

03570083 INSPEC Abstract Number: B90015221, C90022691
Title: Via optimization algorithm of 2-**layer wiring** in VLSI
Author(s): Li Yingmeng; Tang Pushan
Author Affiliation: Dept. of Electron. Eng., Fudan Univ., Shanghai, China
Journal: Chinese Journal of Semiconductors vol.10, no.1 p.31-8
Publication Date: Jan. 1989 Country of Publication: China
CODEN: PTTPDZ ISSN: 0253-4177
Language: Chinese
Abstract: The paper presents a method of looking for the solution of a 2-**layer**-metal-**wiring** via optimization problem. According to topological characteristics and **electrical connectivity**, the wiring is transferred to its equivalent graph with edges weighted in the graph theory. The method is then extended to the case of 3- and 4-linkage via, and redundant vias are introduced to reduce the existing ones still further. Finally an algorithm obtaining the maximum bipartite graph of variable-edge-weight is presented to optimize the 3-/4-linkage vias. The results of the algorithm show that 30%-50% vias can be eliminated.
Subfile: B C

19/3,AB/10 (Item 10 from file: 2)

12/20/2002

DIALOG(R)File 2:INSPEC

03053093 INSPEC Abstract Number: B88007229
Title: Laser-patterned interconnect for thin-film hybrid **wafer**-scale circuits
Author(s): Tuckerman, D.B.
Author Affiliation: Lawrence Livermore Nat. Lab., CA, USA
Journal: IEEE Electron Device Letters vol.EDL-8, no.11 p.540-3
Publication Date: Nov. 1987 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/87/1100-0540$01.00
Language: English
Abstract: A technique is described for **electrically connecting integrated circuit chips** to a silicon **wafer** interconnection substrate, enabling future fabrication of hybrid **wafer** -scale circuits to be performed exclusively with thin-film interconnection technology. Thin-**film wiring** is fabricated down beveled edges of the **chips** and patterned using discretionary laser etching techniques. Interconnections on a 25- mu m pitch (1600 wires around a 1-cm/sup 2/ **chip**) were achieved with this approach. Functioning hybrid memory modules have been fabricated to demonstrate feasibility of the technology.
Subfile: B

19/3,AB/11 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1444580 NTIS Accession Number: DE89009657
Thin-Film **Chip** -to-Substrate Interconnect and Methods for Making Same
(Patent Applicatio)
Tuckerman, D. B.
Lawrence Livermore National Lab., CA.
Corp. Source Codes: 068147000; 9513035
Sponsor: Department of Energy, Washington, DC.
Report No.: PAT-APPL-7-202 296
Filed 6 Jun 88 26p
Languages: English Document Type: Patent
Journal Announcement: GRAI8916; NSA1400
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of application available NTIS. Portions of this document are illegible in microfiche products.
NTIS Prices: PC A03/MF A01
Integrated circuit chips are **electrically connected** to a silicon **wafer** interconnection substrate. Thin **film wiring** is fabricated down bevelled edges of the **chips** . A subtractive wire fabrication method uses a series of masks and etching steps to form wires in a metal layer. An additive method direct laser writes or deposits very thin lines which can then be plated up to form wires. A quasi-additive or subtractive/additive method forms a pattern of trenches to expose a metal surface which can nucleate subsequent electrolytic deposition of wires. Low inductance interconnections on a 25 micron pitch (1600 wires on a 1 cm square **chip**) can be produced. The thin film hybrid interconnect eliminates solder joints or welds, and minimizes the levels of metallization. Advantages include good electrical properties, very high wiring density, excellent backside contact, compactness, and high thermal and mechanical reliability. 6 figs. (ERA citation 14:022847)

19/3,AB/12 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1417081 NTIS Accession Number: DE89000194
Test Probe for Surface Mounted Leadless **Chip** Carrier (Patent Applicatio)
Meyer, K. L. ; Topolewski, J.
Allied Corp., Kansas City, MO. Bendix Kansas City Div.
Corp. Source Codes: 083941001; 9519311
Sponsor: Department of Energy, Washington, DC.
Report No.: PAT-APPL-7-103 865
Filed 2 Oct 87 14p
Languages: English Document Type: Patent
Journal Announcement: GRAI8908; NSA1300
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of application available NTIS. Portions of this document are illegible in microfiche products.
NTIS Prices: PC A03/MF A01
A test probe for a surface mounted leadless **chip** carrier is disclosed. The probe includes specially designed connector pins which allow size reductions in the probe. A thermoplastic housing provides spring action to ensure good mechanical and electrical contact between the pins and the contact strips of a leadless **chip** carrier. Other features include **flexible wires** molded into the housing and two different types of pins alternately placed in the housing. These features allow fabrication of a smaller and simpler test probe. 1 fig. (ERA citation 13:057249)

19/3,AB/13 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05676134
E.I. No: EIP00105364263
Title: Pattern metallization on diamond thick film substrate
Author: Wang, Jiayu; Chen, Hongyu; Bai, Yizhen; Lu, Xianyi; Jin, Zengsun
Corporate Source: Jilin Univ, Changchun, China
Conference Title: 5th International Conference on Advanced Materials
Conference Location: Beijing, China Conference Date: 19990613-19990618
E.I. Conference No.: 57381
Source: Diamond and Related Materials v 9 n 9 Sep 2000. p 1632-1635
Publication Year: 2000
CODEN: DRMTE3 ISSN: 0925-9635
Language: English
Abstract: Diamond thick film with high thermal conductivity and high electrical resistivity has been synthesized with DC-hot cathode PCVD and EA-CVD methods. After being cut, polished and cleaned, diamond thick film was used as electronic packaging material. Pattern metallization on diamond thick film substrates was obtained using a thick-film-writing process. Transition metal ink was directly written on the diamond substrate as base ink. Then gold ink was printed on the transition metal ink. After pre-firing in the atmosphere at 450 degree C for 10 min, the substrate was fired in a vacuum (1.33 Pa) at 850 degree C for 30 min. Minimal or no gold blistering was observed from the fired diamond substrate, and the gold layer had not peeled after several heat impacts (25 approx. 450 degree C). The result indicates that the fired metallization pattern has good adhesion to the diamond substrate. The **chips** were welded easily to the

substrate and further **electrically connected** to the ground, power and signal **layers**, respectively, by **wire** bonding. The surface of the metallized substrate was characterized by scanning electron microscopy (SEM) and the carbide layer was analyzed by X-ray diffraction (XRD). (Author abstract) 5 Refs.

19/3,AB/14 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04154916
E.I. No: EIP95052697526
Title: Present and future directions for multichip module technologies
Author: Sudo, Toshio
Corporate Source: Toshiba Corp, Kawasaki, Jpn
Source: IEEE Journal of Solid-State Circuits v 30 n 4 Apr 1995. p 436-442
Publication Year: 1995
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: Multichip modules (MCM's) have been actively developed in recent years. They are expected to provide high-performance systems by packing bare **chips** at a high density. In particular, a thin-film interconnect substrate that can accommodate higher wiring capacity in a few layers is a new option for coping with high pin count and fine pad pitch VLSI's. MCM's require various kinds of technologies including the fabrication processes of interconnect substrates, **chip connection** methods, **electrical** design, thermal management, known good **die** (KGD), and so on. The state of the art of MCM technologies is reviewed and future directions are discussed. (Author abstract) 21 Refs.

19/3,AB/15 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02653244
E.I. Monthly No: EI8810096866
Title: THICKFILM CIRCUITS WITH GaAsIC: PROTOTYPE MANUFACTURING OF DIGITAL HYBRID CIRCUITS WITH WIREBONDED GaAsIC.
Author: Jorgensen, Tom
Source: Elektronikcentralen (Report) ECR 215 May 1988 69p
Publication Year: 1988
CODEN: ELKRDN
Language: English
Abstract: Mounting of GaAs **IC**'s for high frequencies above 1 GHz has successfully been performed with thermocompression wedge/wedge wire bonding of the **IC**'s to multilayer thickfilm circuits with filled vias and printed resistors. The influence of the bonding wires on the circuit performance was reduced by bonding at least two wires per **IC** -terminal, and further by developing a two-layer substrate technique with 'put-through holes' in the top substrate for the GaAs **chip** which is mounted on the bottom or ground substrate. This has resulted in bonding wires between GaAs **chip** and substrate as short as 0. 3 mm. Silver filled glue was used for the **die** attachment and **electrical connection** of ceramic **chip** capacitors and SMA-connector pins. The mounted substrate was glued to a heat sink and surrounded by a connector holder frame for the connectors. (Author abstract)

19/3,AB/16 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00447268
E.I. Monthly No: EI7504024331
E.I. Yearly No: EI75038249
Title: TEMPERATURE EFFECTS ON THE CHARACTERISTICS OF A JOINT MADE BY ULTRASONIC WELDING BETWEEN AN ALUMINUM **WIRE** AND A **FILM**.
Author: Grachev, A. A.; Pastushenko, A. M.
Source: Russian Ultrasonics v 4 n 3 Jul-Aug 1974 p 95-99
Publication Year: 1974
CODEN: RSUSAR ISSN: 0048-8828
Language: ENGLISH
Abstract: Ultrasonic welding is used in the assembly of **integrated circuits** and semiconductor devices. However, the effect of various temperature loads which could change the properties of the connections during actual use must be considered. In this context, the mechanical and **electrical** properties of **joints** between aluminum **wires** and metal **films** of various thicknesses, after the action of high temperatures and cyclic and continuous heating, are studied. 8 refs.

19/3,AB/17 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03577154 JICST ACCESSION NUMBER: 98A0283431 FILE SEGMENT: JICST-E
Semiconductor devices.
TANAKA KAZUYASU (1); KUROSAWA TETSUYA (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1998, VOL.16,NO.11, PAGE.91-94, FIG.2
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: In an **electrical connection** of the conventional **wire** bonding, multi **layer** formation is difficult which superimposes many **chips**. In a semiconductor equipment which makes connection of a printed wiring board including a multi-**layer wiring** board and silicon **chips** by metal plating, the titled equipment makes wiring of the most front layer by plating, vapor deposition and metal paste, makes electrical wiring board by drilling and plating together and realizes multi layer formation of silicon **chips**. Since wire bonding is not carried out, following merits are obtained.1) Shortening of time.2) Thin semiconductor device.3) High-density wiring.4) Change of layout of pattern wiring is easy.

19/3,AB/18 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01329160 JICST ACCESSION NUMBER: 91A0746914 FILE SEGMENT: JICST-E
Special Issue on Advanced Packagin g Technology for Microelectronics Manufacturing. A Subminiature CCD Module Using a New Assembly Technique.
KONDOH Y (1); SAITO M (1)
(1) TOSHIBA CORP., Kawasaki-shi, JPN

IEICE Trans(Inst Electron Inf Commun Eng), 1991, VOL.E74,NO.8,
PAGE.2355-2361, FIG.11, TBL.6, REF.4
JOURNAL NUMBER: F0699BCQ ISSN NO: 0917-1673
UNIVERSAL DECIMAL CLASSIFICATION: 621.382:537.222
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Electronic video cameras have recently become both small and light. A CCD module is one of the principal devices in electronic video cameras, so it has been requested to become smaller and lighter. The authors have developed a subminiature CCD module. In this subminiature CCD module, a bare CCD **chip** is mounted directly on an optical glass substrate, and the outer circuit is connected to the surface of the glass substrate. This work needs two important assembly techniques. One is the COG wireless bonding technique, and the other is the glass outerconnecting technique. In the COG bonding technique, gold bumps are formed on aluminum pads of a CCD **chip** using the ball bonding method. A thick gold **film wiring** pattern and indium-alloy bumps are formed on the glass substrate. The CCD **chip** is pressed onto the glass substrate, and is heated. The CCD **chip** is **connected electrically** to the glass substrate. The glass outerconnecting technique is that of connecting an FPC(flexible printed circuit) to the glass substrate. The authors decided to use ACF(anisotropic conductive film) connection. An ACF is an adhesive film which has anisotropic conductivity. When it is placed between the glass substrates and FPC, pressed, and heated, the wiring pattern on the glass substrate is connected selectively to the corresponding electrode on the FPC. Four kinds of ACFs were examined and one of them was selected. The optimum conditions for COG wireless bonding and ACF connection using the above selected ACFs were respectively obtained. Four kinds of reliability tests, i.e., a high temperature test, low temperature test, high temperature and high humidity test, and thermal shock test, were carried out for COG bonding and ACF connection. Both COG bonding and ACF connection passed all the four reliability tests. The authors manufactured a subminiature CCD module using these new assembly technique on trial. (abridged author abst.)

19/3,AB/19 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

10387521 PASCAL No.: 92-0590994
Development of a **coated wire** bonding technology
OKIKAWA S; TANIMOTO M; WATANABE H; MIKINO H; KANEDA T
Hitachi Ltd, IC package eng. dep., Kadeira-shi Tokyo, Japan
Electronic components conference, 39 (Houston TX USA) 1989-05-22
Journal: IEEE transactions on components, hybrids, and manufacturing technology; IEEE transactions on components, hybrids, and manufacturing technology, 1989, 12 (4) 603-608
Language: English

19/3,AB/20 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

02964613 PASCAL No.: 80-0244345
ULTRASONIC BALL/WEDGE BONDING OF ALUMINIUM WIRES
(SOUDAGE PAR ULTRASONS DE FILS D'ALUMINIUM "BALL/WEDGE")

12/20/2002

DAWES C J; JOHNSON K I; SCOTT M H
WELDING INST.,ABINGTON CAMBRIDGE CB1 6AL,UNITED KINGDOM
EUROPEAN HYBRID MICROELECTRONICS CONFERENCE. 2/1978/GHENT
1979 379-392
Publisher: PIJNACKER: DUTCH EFFICIENCY BUREAU
Language: ENGLISH
POUR LE SOUDAGE DE FILS FIN EN ALLIAGE ALSI 1% ON FORME UNE BOULE A L'EXTREMITE DU FIL, PAR DECHARGE DE CONDENSATEUR. DESCRIPTION DU PROCEDE ET ESSAIS SUR LES SOUDURES AINSI REALISEES SUR COUCHES MINCES D'ALUMINIUM, D'ALLIAGE PDAG ET D'OR

19/3,AB/21 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

01693154 EDB-86-011711
Author(s): Berglund, C.O.
Title: Seismic apparatus
Patent No.: US 4517664
Patent Assignee(s): Teledyne Exploration Co.
Patent Date Filed: Filed date 12 Nov 1981
Publication Date: 14 May 1985
p v
Language: English
Abstract: A seismic streamer section includes a flexible tube with bulkheads at intervals therealong, end means to make **electrical** and mechanical **connections** with adjacent sections, tension lines extending from one end to the other through the bulkheads, hydrophones in the tube between the bulkheads, an electric bundle including through conductors extending from one end means to the other through the bulkheads to various ones of the hydrophone. Each hydrophone comprises a drum shaped case with dished ends and convex sides providing standoff from the bundle and lines for piezoelectric **wafers** supported inside the ends. A cylindrical metal ring forms the side of the case. Stainless steel cups disposed with their bottoms adjacent and having their rims welded to the rims of the ring form the ends of the case. The piezoelectric **wafers** are conductively secured one each to the inner surfaces of flexible diaphragms forming the bottoms of the cups. Flat metal discs are conductively secured one each to the mid-portions of the adjacent faces of the **wafers**. **Flexible** metal **wires** are integrally connected one each at one end to the outer peripheries of the discs. The other ends of the wires are inserted into and soldered to a metal tube extending radially through the ring. The tube is ceramically insulated from the ring and sealed thereto fluid tight. The tube may be bonded in place to the ring. The metal discs are separated by a distance equal to the sum of the permissible maximum inward displacements of the **wafers**. An elastomeric bumper may surround the ring.

25/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

02109021 INSPEC Abstract Number: B83048876
Title: Microjoining developments for the electronics industry
Author(s): Johnson, K.I.
Author Affiliation: Welding Res. Inst., Abingdon, UK
Journal: Hybrid Circuits no.2 p.5-11
Publication Date: Spring 1983 Country of Publication: UK
CODEN: HYCRD5 ISSN: 0265-3028
Language: English
Abstract: Describes the major microjoining developments currently of interest to the microelectronics industry, with emphasis on the work conducted by the microjoining section of the Welding Institute, much of which has been directly sponsored by the UK Ministry of Defence (DCVD). The author discusses two welding operations; making **electrical connections** to **solid state** transistor or integrated silicon circuits; fabricating packages and devices containing such **solid state** circuits and passive devices (resistors, capacitors, conductors).
Subfile: B

25/3,AB/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

2108350 NTIS Accession Number: DE98002810/XAB
Mechanical properties of Pb-free solder alloys on thick film hybrid **microcircuits**
Hernandez, C. L. ; Vianco, P. T. ; Rejent, J. A. ; Hosking, F. M.
USDOE, Washington, DC.
Corp. Source Codes: 888888888
Report No.: SAND-97-2578C; CONF-980422
10 Mar 98 10p
Languages: English Document Type: Conference proceeding
Journal Announcement: GRAI9908; ERA9902
IPC printed circuits expo '98.
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NTIS Prices: PC A02/MF A01
The technology drivers of the electronics industry continue to be systems miniaturization and reliability, in addition to addressing a variety of important environmental issues. Although the Sn-Pb eutectic alloy is widely used as a joining material in the electronics industry, it has drawn environmental concern due to its Pb content. The solder acts both as an **electrical** and mechanical **connection** within the different packaging levels in an electronic device. New Pb-free solders are being developed at Sandia National Laboratories. The alloys are based on the Sn-Ag alloy, having Bi and Au additions. Prototype hybrid **microcircuit** (HMC) test vehicles have been assembled to evaluate Pb-free solders for Au-Pt-Pd thick film soldering. The test components consist of a variety of dummy **chip** capacitors and leadless ceramic **chip** carriers (LCCC's). The mechanical properties of the joints were evaluated. The reflow profiles and the **solid state** intermetallic formation reaction will also be presented. Improved solder joint manufacturability and increased fatigue resistance solder alloys are

the goals of these materials.

25/3,AB/3 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

0543591 NTIS Accession Number: AD-D002 198/0/XAB
Method of Producing Current with Ceramic Ferroelectric Device (Patent)
Brody, P. S.
Department of the Army Washington D C
Corp. Source Codes: 109900
Report No.: PAT-APPL-411 853; PATENT-3 855 004
Filed 1 Nov 73 patented 17 Dec 74 7p
Document Type: Patent
Journal Announcement: GRAI7610
Supersedes PAT-APPL-411 853.
Government-owned invention available for licensing. Copy of patent available Commissioner of Patents, Washington, D.C. 20231 $0.50.
NTIS Prices: Not available NTIS
The patent relates to a device which consists of a **wafer** of polycrystalline perovskite oxide ceramic such as barium titanate, **lead** titanate - **lead** zirconate, or **lead** titanate-**lead** zirconate with 7.5% or less of the **lead** substituted for by lanthanum. **Electrical** terminals are **joined** to the **wafer** edges. When the ceramic is exposed to visible radiation such as sunlight a high voltage appears across the terminals and an electrical current flows through a load resistance connected between said terminals. The voltage across the load resistance depends upon the length of the **wafer** between the two terminals and the magnitude of the load resistance. Voltages of at least 500 volts per inch are produced for high values of load resistance.

25/3,AB/4 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03043514 JICST ACCESSION NUMBER: 97A0159470 FILE SEGMENT: JICST-E
Structure and Characteristics of BCC.
SAKODA HIDEHARU (1); TSUJI KAZUTO (1); ORIMO SEIICHI (1); NOMOTO RYUJI (1); ONODERA MASANORI (1); YONEDA YOSHIYUKI (1); KASAI JUN'ICHI (1)
(1) Fujitsu Ltd.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1996, VOL.96,NO.416(ICD96 160-167), PAGE.9-15, FIG.21, TBL.2, REF.5
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: BCC(Bump **Chip** Carrier) we developed as one form of the low pin-count CSP(**Chip** Scale Package) uses the half-etching proceeded leadframe as the base material. In the etching process, it is removed and the terminal (resin bump) is formed. Au wire and Pd plating layer were applied for **electrical connection** between LSI **chip** and the terminal. BCC16 has already been in a practical stage, and because not only of its smaller size but has no problem of **lead** bending, it is expected as the replacement of SSOP and COB

in the future. This paper describes the reliability of BCC (Solderability, mountability etc) and the influence of leadless on its characteristics (electrical characterestics, thermal resistance etc). (author abst.)

25/3,AB/5 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02678896 JICST ACCESSION NUMBER: 96A0299604 FILE SEGMENT: JICST-E
Investigation of Cu wire stitch bonding. (Report 1). Influence of bonding condition and surface state on bondability.
FUJIMOTO KOZO (1); MANABE TOSHIKI (1); NAKATA SHUJI (1); FUJII ATSUHIKO (2)
(1) Osaka Univ.; (2) Sumitomo Electr. Ind., Ltd.
Yosetsu Gakkai Ronbunshu(Quarterly Journal of the Japan Welding Society), 1996, VOL.14,NO.1, PAGE.168-173, FIG.13, TBL.1, REF.7
JOURNAL NUMBER: Y0413AAA ISSN NO: 0288-4771
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2 669:621.791
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Wire bonding is used as a method of the **electrical connections** between an electrode terminal on a **chip** of a semiconductor and an outer **lead** terminal. Cu wire has a good corrosion resistance and high electrical and thermal conductivity. Furthermore, Cu wire can be bonded directly to Cu alloy **lead** frame as a 2nd stitch bonding. For these reasons, a practical application of the Cu wire bonding process is anticipated. But, for application of Cu wire stitch bonding onto Cu alloy **lead** frame, there are a lot of difficult problems to be solved. In this report, the influence of the bonding conditions and surface states on the bondability of Cu wire stitch bonding is investigated. It is pointed out that the control of the wire deformation behavior is necessary for obtaining the good bondability in thermosonic Cu wire bonding. Furthermore, it is clarified that the surface state on Cu alloy **lead** affects on the bondability. If the maximum surface roughness on Cu alloy **lead** is more than 0.4.MU.m, or if the thickness of the oxide film on Cu alloy **lead** is more than 10nm, the bondability of Cu wire stitch bonding is inferior. (author abst.)

25/3,AB/6 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02545505 JICST ACCESSION NUMBER: 95A0396405 FILE SEGMENT: JICST-E
Bonding wire.
CHIBA NOBUYUKI (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1995, VOL.13,NO.25, PAGE.101-104, FIG.5
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The bonding wire for conventional **integrated circuit** is formed in single track. When it is used for connection **integrated circuit** element and leadframe, and if there is

any breakage in the wire, there will be no **electrical connection**. And, it is not resistant to mechanical stress. In this technology plural bonding wires are used to couple **integrated circuit** element with leadframe, mechanical stress is dispersed, and the reliability is ensured by strengthening mechanical combination and electric link.

25/3,AB/7 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00744172 JICST ACCESSION NUMBER: 89A0458950 FILE SEGMENT: JICST-E
Large-size contact-type **image** sensor.
MURATA TAKAHIKO (1); SHIRAISHI TSUKASA (1); FUJIWARA SHINJI (1)
(1) Matsushita Electronic Component Co., Ltd., Electronic Component Lab.
Natl Tech Rep, 1989, VOL.35,NO.4, PAGE.394-399, FIG.10, TBL.5, REF.3
JOURNAL NUMBER: G0474AAH ISSN NO: 0028-0291 CODEN: NTROA
UNIVERSAL DECIMAL CLASSIFICATION: 621.397.61 681.3:621.397.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A high-resolution large-size contact-type **image** sensor has been developed for reading large-size drawings and printed circuit boards. It employs barium borosilicate glass for the mounting substrate, which makes possible large size and low stress applied to the silicon **chip**. By means of the full-cut dicing from the back of the silicon **wafer** in addition to the half-cut dicing, and the **die**-bonding used for heat-hardening from the back of the substrate, the accuracy of the **chip** connection has been improved. The A0-size contact-type **image** sensor has a resolutioon of 400 DPI(dots per inch), and a reading length of 853.4mm. It is of the in-line type which requires no optical **connection** and **electrical connection**. The stress applied to the **image** sensor **chip** has been reduced to 1/5, which improves the reliability. Also, the accuracy of the **chip** connection is within 1.5.MU.m, which improves the reading quality.(author abst.)

25/3,AB/8 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15325076 PASCAL No.: 02-0010819
Alternatives for joining Si **wafers** to strain-accommodating Cu for high-power electronics
FAUST Nicholas; MESSLER Robert W JR; KHATRI Subhash
Howmet, Whitehall, MI, United States; Silicon Power Corporation, Malvern, PA, United States
Journal: Journal of electronic materials, 2001, 30 (10) 1276-1286
Language: English
Differences in the coefficients of thermal expansion (CTE) between silicon **wafers** and underlying copper electrodes have led to the use of purely mechanical dry pressure contacts for primary **electrical** and thermal **connections** in high-power **solid-state** electronic devices. These contacts are limited by their ability to dissipate I SUP 2 R heat from within the device and by their thermal fatigue life. To increase heat dissipation and effectively deal with the CTE mismatch, metallurgical bonding of the silicon to a specially-structured, strain-accommodating copper electrode has been proposed. This study was intended to seek

alternative methods for and demonstrate the feasibility of bonding Si to structured Cu in high-power **solid-state** devices. Three different but fundamentally related fluxless approaches identified and preliminarily assessed were: (1) conventional Sn-Ag eutectic solder; (2) a new, commercially-available active solder based on the Sn-Ag eutectic; and (3) solid-liquid interdiffusion bonding using the Au-In system. Metallurgical joints were made with varying quality levels (according to nondestructive ultrasonic C-scan mapping, SEM, and electron microprobe) using each approach. Mechanical shear testing resulted in cohesive failure within the Si or the filler alloys. The best approach, in which eutectic Sn-Ag solder in pre-alloyed foil form was employed on Si and Cu substrates metallized (from the substrate outward) with Ti, Ni and Au, exhibited joint thermal conduction 74% better than dry pressure contacts.

25/3,AB/9 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

07327330 PASCAL No.: 86-0327768
Extended abstracts of the 16th international conference on **solid state** devices and materials, Kobe, August 30-September 1, 1984
Japan Society of Applied Physics, Tokyo, Japan; IEEE. Electron Devices Society, New York NY, USA
International conference on solid state devices and materials. 16 (Kobe) 1984-08-30
1984 2 vol., IX-721 p., XIX-88 p.
Publisher: Japan Society of Applied Physics, Tokyo
Language: ENGLISH

34/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03767091 INSPEC Abstract Number: A91000501
Title: Construction of combined field ion-scanning tunneling microscope and its performances
Author(s): Murakami, K.; Miyao, M.; Nomura, T.; Ishikawa, K.; Hagino, M.; Sasaki, A.; Yamaguchi, T.; Nishino, N.; Fukuoka, S.
Author Affiliation: Res. Inst. of Electron., Shizuoka Univ., Hamamatsu, Japan
Journal: Bulletin of the Research Institute of Electronics, Shizuoka University vol.24, no.2 p.79-90
Publication Date: 1989 Country of Publication: Japan
CODEN: SDDHDM ISSN: 0286-3383
Language: Japanese
Abstract: Recently, an ultra high vacuum (UHV) scanning tunneling microscope (STM) combined with a field ion microscope (FIM) has been constructed. In order to investigate its fundamental performances, a graphite surface and PbTiO/sub 3/ fine particles are observed in air. The STM observations on the graphite surface give an atomically resolved **image** . In the case of the PbTiO/sub 3/ fine particles, the results suggest that it is necessary to consider the conductive materials for **coating** the **insulators**. Finally, the observation of a field ion **image** is carried out on a W probe tip for scanning. The FI **image** shows that the crystal direction of the W tip is (110). The obtained results suggest that the newly constructed field ion-scanning tunneling microscope system is useful for the studies on the various **solid state** and semiconductor reconstructed surfaces.
Subfile: A

34/3,AB/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1805789 NTIS Accession Number: DE94006298
Photoelectron diffraction and holography: Present status and future prospects
Fadley, C. S. ; Thevuthasan, S. ; Kaduwela, A. P.
Lawrence Berkeley Lab., CA.
Corp. Source Codes: 086929000; 9513034
Sponsor: Department of Energy, Washington, DC.
Report No.: LBL-35054; CONF-930764-1
Jul 93 29p
Languages: English Document Type: Conference proceeding
Journal Announcement: GRAI9415; ERA9427
International conference on electron spectroscopy (5th), Kiev (Ukraine), 26 Jul - 1 Aug 1993. Sponsored by Department of Energy, Washington, DC.
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NTIS Prices: PC A03/MF A01
Photoelectron diffraction and photoelectron holography, a newly developed variant of it, can provide a rich range of information concerning surface structure. These methods are sensitive to atomic type, chemical state, and spin state. The theoretical prediction of diffraction patterns is also well developed at both the single scattering and multiple scattering levels, and quantitative fits of experiment to theory can **lead** to structures with

accuracies in the (plus minus)0.03 (Angstrom) range. Direct structural information can also be derived from forward scattering in scanned-angle measurements at higher energies, path length differences contained in scanned-energy data at lower energies, and holographic inversions of data sets spanning some region in angle and energy space. Diffraction can also affect average photoelectron emission depths. **Circular** dichroism in core-level emission can be fruitfully interpreted in terms of photoelectron diffraction theory, as can measurements with spin-resolved core-spectra, and studies of surface magnetic structures and phase transitions should be possible with these methods. Synchrotron radiation is a key element of fully utilizing these techniques.

34/3,AB/3 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1546135 NTIS Accession Number: DE90636629
Heavy-ion irradiation tracks in zircon
Bursill, L. A. ; Braunshausen, G.
Melbourne Univ., Parkville (Australia). School of Physics.
Corp. Source Codes: 007094003; 4066000
Report No.: UM-P-89/105
1989 54p
Languages: English
Journal Announcement: GRAI9104
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NTIS Prices: PC A04/MF A01
Heavy-ion irradiation (14 MeV/u Pb ions) of zircon crystals gives rise to linear latent tracks of 80x10(sup -10) m diameter and length 140 (mu)m. Direct observation of the track core, by high-voltage high-resolution electron microscopy at atomic resolution, reveals a core having roughly **circular** cross-section, with some facetting of the core/matrix interface on (101) planes of zircon. The core diameter appears quite uniform. Conventional transmission electron microscopy (bright- and dark-field imaging) reveals an elastic strain field extending for a short distance into the zircon matrix. This appears to drop off more rapidly with distance, say 1/R(sup 2), than do dislocation strain fields ((approx) 1/R). Analysis of the various contrast mechanisms yields the result that the core is essentially amorphous. The observations confirm directly earlier conclusions based on track etching and electrical conductivity measurements, that the irradiation damage is confirmed to a 50-100 Aangstroem core region of atomically-disordered material, with virtually no damage outside this region. Mechanisms for track production are discussed briefly, but it is concluded that the problem, which is now defined by this structural analysis, has not been fully-appreciated by condensed matter physicists. In particular a damage confinement mechanism is required, which is not intuitively obvious. Some tentative suggestions along this direction are proposed. 33 refs., 9 figs. (Atomindex citation 21:070762)

34/3,AB/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03839159
E.I. No: EIP94041249694
Title: Analysis of time-resolved, in-situ change in high-resolution

electron microscopy
Author: Kang, Z.C.; Eyring, L.
Corporate Source: Arizona State Univ, Tempe, AZ, USA
Conference Title: Proceedings of the John M. Cowley Symposium on Aspects of Electron Microscopy, Difraction, Crystallography and Spectroscopy
Conference Location: Scottsdale, AZ, USA Conference Date: 19930105-19930108
E.I. Conference No.: 19975
Source: Ultramicroscopy v 52 n 3-4 Dec 1993. p 377-382
Publication Year: 1993
CODEN: ULTRD6 ISSN: 0304-3991
Language: English
Abstract: The mechanisms proposed for physical change or for **solid state** chemical reactions are usually couched in phenomenological terms partly because of the difficulty of obtaining detailed information on occurrences at the atomic level. Use of the high-resolution electron microscope could provide the required atomic-level information in those instances where the rate of change is suitable. Two cases where the transformation rates are near the lower time limits of present capability are used here as illustrations. First, the removal of a twin boundary separating a surface promontory from the main body of a TbO//2 crystal is followed and analyzed from sequences of video-field **images** recorded at 1/60 second. Sudden disorder of the promontory is followed within a few seconds by reconstructive, epitaxial, outward growth on the main body of the crystal. Second, to illustrate similar analyses of a chemical reaction, an episode in the transformation of a **lead** zirconate titanate (PZT) precursor gel toward the crystalline PZT is observed at intervals from video-fields selected during condensations and the loss of solvent and the accompanying crystallization process. Areas of condensation on the surface of the colloidal **sphere** are amorphous at first but begin fitful crystallization when the diameter reaches about 3 nm and continues wild reconstructions until the stable perovskite is formed. (Author abstract) 4 Refs.

34/3,AB/5 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04337460 Genuine Article#: BA74Z Number of References: 57
Title: SURFACE-STRUCTURE OF AMORPHOUS AND CRYSTALLINE POROUS SILICAS - STATUS AND PROSPECTS (Abstract Available)
Author(s): UNGER KK
Corporate Source: UNIV MAINZ,INST ANORGAN CHEM & ANALYT CHEM,POB 3980/W-6500 MAINZ//GERMANY/
Journal: ADVANCES IN CHEMISTRY SERIES, 1994, V234, P165-181
ISSN: 0065-2393
Language: ENGLISH Document Type: REVIEW
Abstract: Substantial progress in the elucidation of the surface structure of crystalline and amorphous silicas has been achieved by means of high-resolution spectroscopic techniques, for example, Si-29 cross-polarization magic-angle spinning NMR spectroscopy and Fourier transform IR spectroscopy. The results **lead** to a better understanding of the acidity, dehydration properties, end adsorption behavior of the surface. These properties are key features in the design of novel advanced silica materials. The current methods of characterization are briefly reviewed and summarized.

34/3,AB/6 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

12/20/2002

01623958 AAD9819504
SIMULATION OF NOVEL **SOLID STATE** COLD CATHODE STRUCTURES (ELECTRON EMISSION, MICROWAVE TUBE)
Author: MUMFORD, PHILIP DOUGLAS
Degree: PH.D.
Year: 1997
Corporate Source/Institution: UNIVERSITY OF CINCINNATI (0045)
Source: VOLUME 58/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 6734. 148 PAGES

The development of innovative electron emitter materials, structures, and devices is needed to support evolving vacuum electronic technologies to satisfy future requirements for microwave tube sources. Advanced emitter devices which support the spatial and temporal modulation of a high current density electron source attack these requirements directly. Use of materials engineering to tailor the internal electronic structure of a device along with advanced microfabrication capabilities to define precise geometric features enables the controlled injection, transport, and emission of electrons in a **solid state** emitter structure.

This thesis describes the design and modeling of a new **solid state** electron emission device. Such a device will be capable of emission current densities up to 100 A/$cm\sp2$ with a total current of up to several amps for primary use in microwave power amplifier tubes. This type of electron emitter does not need to be heated above room temperature as is the case for a thermionic cathode and is referred to as a cold cathode.

In this thesis, simulations of electron transport in an $AlGaN/GaN/LaB\sb6$ **solid state** cold cathode and guidelines for the design of a $Metal/CdS/LaS$ based cold electron emitter are presented. Our analysis provides the basic design rules to fabricate a new cold cathode with emission windows of a rectangular or **circular** geometry. The growth of the structure would require the epitaxial growth of both CdS and LaS layers. As discussed in the thesis, the epitaxial growth of InP/CdS heterostructures has been reported in the literature but deposition of epitaxial LaS thin films has not been reported, to the best of our knowledge. We believe, however, that the figures of merits of the various cold cathodes analyzed in this work are a strong incentive towards the experimental investigation of these devices. If successful, such an experimental effort would **lead** to big pay-offs with the design of highly efficient cold cathodes for large flat panel displays, IR **image** convertors and sensors, and active power devices in mobile and airborne electronic equipment for military, commercial, and private use.

34/3,AB/7 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01400750 AAD9506940
SCANNING PROBE MICROSCOPY STUDIES OF SURFACE AND ELECTRONIC STRUCTURES IN LOWER-DIMENSIONAL METALS AND INSULATORS
Author: XUE, QING
Degree: PH.D.
Year: 1994
Corporate Source/Institution: UNIVERSITY OF VIRGINIA (0246)
Source: VOLUME 55/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 4446. 245 PAGES

A scanning tunneling microscope (STM) and atomic force microscope

(AFM) operating under ambient conditions have been used to study surface and electronic structures of various crystals described in this dissertation.

The intercalation of Fe in the 2H phase transition-metal dichalcogenides produces many interesting features. At high concentration, the Fe becomes ordered in the octahedral holes in the van der Waals gap, and superlattices of the form 2${\bf a}\sb0 \times 2{\bf a}\sb0$ and $\sqrt{3{\bf a}}\sb0 \times \sqrt{3{\bf a}}\sb0$ are observed with both the STM and AFM. It is also detected with the AFM scans that the interstitial impurities such as Mn and Cr induce long range charge modulations in NbSe$\sb3$ at room temperature. The wavelengths of modulation are functions of the impurity concentration. It is unique to the one-dimensional chain structure and is related to the existence of anomalies of the electric susceptibility which **lead** to the CDW formation at low temperature. A sudden change in crystal structure in Cr$\rm\sb{0.05}NbSe\sb3$ is also observed which shows a metal-insulator transition and the crystal is insulating at room temperature.

The AFM has been used to study the surface of mica before and after etching. Before etching, scans show that alternating oxygen atoms in the hexagonal rings differ in height. After etching, the AFM measurements show the rate of growth of etchpit depth is faster for alpha-recoils than for cesium ions. The oxidized and reduced Fe $\{$100$\}$ surfaces have also been studied using the STM and AFM. The surfaces have been **imaged** under ambient conditions after preparation using hot hydrogen anneals either before or after oxidizing at high temperature. The extremely low tunnel barrier allows the STM to be used for study of the internal structure of thick **oxide layers** while the AFM can be used to study the topography of the surface layer.

Naturally occurring defects down to a single atom vacancies can be observed with both the STM and AFM although atomic defects seem to be absent in a number of AFM scans. In addition, defects can also be introduced into the surface of crystal using either the STM and AFM. The dimensions of the defects are determined by the size of the voltage pulse in the case of the STM or the force applied to the AFM tip.

34/3,AB/8 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01239788 AAD9226700
THEORY OF ELECTRON EMISSION FROM ATOMICALLY SHARP METALLIC EMITTERS IN HIGH ELECTRIC FIELDS (METALLIC EMITTERS)

Author: HE, JUN
Degree: PH.D.
Year: 1992
Corporate Source/Institution: THE PENNSYLVANIA STATE UNIVERSITY (0176)
Source: VOLUME 53/05-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 2381. 172 PAGES

A systematic theoretical investigation of the effect of tip geometry on the field emission current voltage characteristics from atomically sharp metallic field emitters is presented. A free electron model is used for the metal emitters with non-planar geometries in studying the dependence of the current density on tip geometry, local field, and temperature. To construct the surface potential barriers, the classical **image** interaction is derived exactly for the metal emitters modeled as cones, paraboloids, hyperboloids and **sphere** on cones. Numerical results show that the classical **image** interaction for these non-planar emitter geometries is diminished in magnitude relative to the planar **image** interaction. It is found that the bias potential for the model emitter significantly

modifies the shape of the tunneling barriers, and the resulting form predicts a dramatically enhanced current relative to the classical Fowler-Nordheim result.

The transmission coefficients for the surface potential barriers are evaluated within the WKB approximation. The current-voltage characteristics are then calculated for these models using the kinetic formulation of the current density integral. The calculated results, plotted as log J/V$\sp2$ vs. 1/V, do not exhibit the straight line behavior predicted by the Fowler-Nordheim model for field emission from a planar surface. The effects of emitter curvature on electron emission in combined high fields and elevated temperature are also examined.

An approximate analytic expression for the J(V) characteristics of a prototype sharp emitter is derived which exhibits explicitly the dependence of the current density on geometric and material parameters.

The adequacy of a β-factor in the conventional planar model F-N equation to account for emitter curvature is examined. It is demonstrated that the use of such an F-N equation is incorrect when applied to sharp emitters (r$\sb{\rm t}\le 10$nm) and will **lead** to spurious results when used to extract information such as field values or emitting area from experimental F-N curves.

Lastly, the effect of tip geometry on the Nottingham energy exchange and temperature stability is studied. The calculated results show that the lower replacement energy yields significant lowering of the inversion temperature. The calculation of current density versus inversion temperature suggests that the non-planar hyperboloidal emitter can be operated at a higher current density.

34/3,AB/9 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01138683 AAD9101915
ELECTRON DIFFRACTION AND MICROSCOPY STUDIES OF SURFACES (ALUMINA, THIN FILMS)

Author: YAO, NAN
Degree: PH.D.
Year: 1990
Corporate Source/Institution: ARIZONA STATE UNIVERSITY (0010)
Source: VOLUME 51/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3920. 277 PAGES

The focus of this dissertation has been devoted to the investigation of the various phenomena observed in surface studies by means of reflection electron microscopy, reflection high energy electron diffraction, and reflection electron energy loss spectroscopy. The aim of this effort is to elucidate the process of interaction between electrons and a crystal lattice in the surface region, and to **lead**, in turn, to a comprehensive understanding of surface structure, surface domain, surface reactions, and surface dynamical processes. The resonance conditions responsible for the enhancement of the specular reflected beam observed in the diffraction from crystal surfaces have been characterized as Bragg-Channelling reflection and Bragg-Bragg reflection, respectively, in terms of different scattering mechanisms. Under these two resonance conditions, the tremendous increase in both elastic and inelastic electron scattering results in an intensity enhancement of the specular reflected beam. The parabolas and **circles** observed in diffraction patterns from crystal surfaces are closely associated with the electron channelling in the surface region. For the higher electron energy, the levels of the surface bound states go down deeper into the potential wells of rows of atoms. There is a strong temperature dependence on both surface channelling

and normal reflected electrons. The total reflectivity did not change considerably with the variation of the diffraction condition. The improvement of the topographical contrast in surface imaging was not simply related to the increase in the intensity of the specular reflected beam. The surface **image** obtained from the Bragg-Bragg reflection condition showed a better **image** contrast for the surface structure among the varieties of resonance conditions. The appearances of the abnormal double contour contrast for a single-atom height step, which can be observed mostly with the fulfillment of the Bragg-Bragg reflection condition, was attributed to the electron dynamical scattering related to the surface channelling effect. The surface **image** contrast for the surface steps and dislocations were studied in detail under a variety of experimental conditions. Thin film specimens were prepared by depositing gold on GaAs and InP (110) surfaces. The epitaxial relationship and the interface reaction mechanisms were studied in detail. A new method of preparing atomic flat surfaces of copper single crystals with all possible lattice planes was developed. The surface oxides formed from the oxygen present in the bulk copper as Cu$\sb2$O inclusion were not found in this case.

Detailed investigations of surface atomic structure, surface reactions with oxygen on α-Alumina single crystal (0, -1, 1) facets, and the surface domains with O-rich, and Al-rich termination are presented.

34/3,AB/10 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03646539 JICST ACCESSION NUMBER: 98A0672552 FILE SEGMENT: JICST-E
Control of Ball and Plate Game using Tracking Vision.
NAGATA SHIGEYUKI (1); KUME HIROSHI (2)
(1) Tokushima Bunri Univ.; (2) Tokushimabunridai Daigakuin
Tokushima Bunri Daigaku Kenkyu Kiyo(Technical Bulletin of Tokushima Bunri University), 1997, NO.54, PAGE.69-77, FIG.16, REF.9
JOURNAL NUMBER: Z0788AAG ISSN NO: 0286-9829
UNIVERSAL DECIMAL CLASSIFICATION: 007.52:681.51
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: It is very difficult for robots to walk bipedally, to take something by looking, to catch moving objects and so on, all of which are very easy for humans to do. We, humans, recognizing the environment by senses of sight and hearing, for example, can predict the result and decide to act. Therefore, it is very interesting to research making robots do human actions. We mainly recognize the environment by the sense of sight. Our studies were conducted about how to have a robot play the ball-and-plate game in which the robot is supposed to not drop the ball from the plate using information from a CCD camera. In our previous system, we processed **images** from a CCD camera to detect the ball's position and followed by calculating the distance from the center of the plate. Then we inclined the plate in proportion to the distance. Because of long **image**-processing time, it is impossible to detect the ball's position in real time. In this work we used a tracking vision instead, which is a high-speed calculating tracking apparatus and is able to output the information of positions of plural moving targets continuously at the video rate. In order to have a robot play the ball-and-plate game, consider how a human being would play the game. First, he confirms the condition of the ball on the plate. He recognizes the position and the velocity of the ball, and he inclines the plate to **lead** the ball toward the center of the plate. When the ball is drawn near to the target point, he adjusts the inclination

of the plate so that the ball may stop at the target point. When the ball reaches the target point, he makes the plate horizontal. The algorithm of our program is based on the above conception. As the result, we can make a robot simulate the human movement of the game. However, sometimes the ball dropped off the plate, because we decided empirically the parameters to send to the robot, which may not be optimal. (author abst.)

34/3,AB/11 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03589055 JICST ACCESSION NUMBER: 98A0635280 FILE SEGMENT: JICST-E
Microwave and Millimeter-Wave Module Technology. Miniaturized Front-End HIC Using MBB Technology for Mobile Communication Equipment.
ITOH J (1); NAKATSUKA T (1); YOSHIDA T (1); NISHITSUJI M (1); UDA T (1); ISHIKAWA O (1)
(1) Matsushita Electronics Corp., Moriguchi-shi, JPN
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1998, VOL.E81-C,NO.6, PAGE.834-840, FIG.14, TBL.2, REF.9
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Highly miniaturization technology in frontend GaAs Hybrid IC for mobile communication equipment will be presented. A combination of MBB (micro bump bonding) technology and the new GaAs IC fabrication process using high dielectric constant (.EPSILON.r) thin film technology has achieved a super small HIC with low cost and low power consumption. The new HIC was constructed of only a ceramic substrate in which the spiral inductors were formed on it and the GaAs IC chip that was bonded by using MBB technology. The MBB technology **lead** the HIC to a lower temperature process without soldering, a smaller bump diameter, at shorter intervals and the lowest parasitic in the bump. The advantage of the small bonding pad of the IC contributes to miniaturize the IC chip and reduces the chip cost. The GaAs IC process technology using high-.EPSILON.r thin film achieves the integration of all capacitors in the IC without increasing the chip size. Furthermore, low power consumption was achieved by 0.5-.MU.m LDD BP-MESFET with a high k-value. Although capacitors were integrated on the IC, all of the inductors were formed on the top of the ceramic substrate using a thin film metal process. This was used due to its large occupation area when it was integrated on the IC, and produced a low Q-factor. As a results, the chip was minimized to a size of 0.8 * 1.0 mm2 and achieved a low-cost chip. Two types of HICs were fabricated for 880 MHz cellular band and 1.9GHz PHS (Personal Handy phone System) band. The HIC at 880 MHz measures only 5.0 * 5.0 * 1.0 mm3, and offered a conversion gain of 25 dB, a noise figure of 4.2 dB and an **image** rejection ratio of 12 dB at 2.7 V and at a power supply of 3.5 mA. The HIC for 1.9 GHz measures only 3.5 * 4.0 * 1.0 mm3, and showed a conversion gain of 16.0dB, a II P3 of -16.0dBm, and an **image** rejection ratio of over 20 dBc at 3.0 V and at power supply of 4.5 mA. (author abst.)

34/3,AB/12 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

12/20/2002

03522577 JICST ACCESSION NUMBER: 98A0047826 FILE SEGMENT: JICST-E
'98 Latest semiconductor process technology. Technology & Equipment. Metallization process technology. Metallization process technology for the age of 300mm/0.18 .MU.m.
SHIBATA HIDEKI (1)
(1) Toshiba Corp.
Gekkan Semiconductor World(Semiconductor World), 1997, VOL.16,NO.14, PAGE.241-246, FIG.9, REF.12
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper discusses problems caused by the miniaturization of contact electrodes as follows; the trends and issues of metallic thin film formation technology, the necessity of innovation to dmascene technology, the trends and issues of damascene wiring formation technology and multi-**layer wiring** structures in the 0.18.MU.m generation. With regards to multi-**layer wiring** structures of the 0.18.MU.m generation, the problems will arise to technologies introduced up to the 0.25.MU.m generation. The solution of these problems requires the innovation to dual damascene technology which embeds wiring and connection holes simultaneously with the same material. Based on the discussions thus far, this paper shows an **image** of a siz **layer wiring** cross section in the 0.18.MU.m generation. For its realization, the development of film formation technology becomes very important in order to embed Al and Cu uniformly in ducts with aspect more than. It shows that the formation of metallic thin films less than 10nm will become very important from now on.

34/3,AB/13 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03470889 JICST ACCESSION NUMBER: 98A0282961 FILE SEGMENT: JICST-E
Microscale Thermal Measurement using the Atomic Force Microscope. 2nd Report, Temperature and Thermophysical Properties Measurement.
NAKABEPPU OSAMU (1); IGETA MASANOBU (2); KAJII MAKOTO (2); HIJIKATA KUNIO (3)
(1) Univ. of Tokyo; (2) Tokyo Inst. of Technology, Graduate School; (3) Tokyo Inst. of Technol. Fac. of Eng.
Nippon Kikai Gakkai Ronbunshu. B(Transactions of the Japan Society of Mechanical Engineers. B), 1998, VOL.64,NO.618, PAGE.549-555, FIG.11, REF.9
JOURNAL NUMBER: F0036BAN ISSN NO: 0387-5016
UNIVERSAL DECIMAL CLASSIFICATION: 536.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Experimental study on microscale measurement of temperature and thermophysical properties using the Atomic Force Microscope was conducted. Thermal and topological **images** were taken by scanning a gold **film** on nickel **wire** type thermocouple probe on sample with constant contact load. Visualization of temperature distribution of thin film resistor of 20.MU.m square and thermal conductance distribution of composite material called CFRP were attempted. With reducing ambient gas pressure, heat transfer mode

between the probe and sample changes from gas conduction to solid conduction through contact point, thus contrast of temperature **image** becomes weaker and spatial resolution improves from 30.MU.m to less than 1.MU.m. In the properties measurement, it has been demonstrated that sub-micron scale visualization of thermal conductance is possible by this method and resultant **image** is affected by sample geometry and thermophysical properties distribution. (author abst.)

34/3,AB/14 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03088202 JICST ACCESSION NUMBER: 97A0127381 FILE SEGMENT: JICST-E
Thermal Measurement in Micro-Scale Region using the Atomic Force Microscope.
NAKABEPPU OSAMU (1); HIJIKATA KUNIO (1); IGETA MASANOBU (2); MAJUMDAR A (3)
(1) Tokyo Inst. of Technol. Fac. of Eng.; (2) Tokyo Inst. of Technology, Graduate School; (3) UCSB
Thermophys Prop, 1996, VOL.17th, PAGE.51-54, FIG.7, REF.8
JOURNAL NUMBER: X0031AAB ISSN NO: 0911-1743
UNIVERSAL DECIMAL CLASSIFICATION: 536.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: New technique with the AFM(Atomic Force Microscope) for thermal measurement in microscale beyond light wavelength have been developed. This paper shows experimental research on microscale thermal imaging of biased electric devices by combining small T.C. (thermo-couple) probes and the AFM. Three types of the T.C. cantilever shown in Figs. 2-3 were made and tried. Wire type T.C. probe can be fabricated easily by spot welding of two sharpen metal wires, but its large junction causes to low response. While, thin film type T.C. probe is made through a difficult work of metal vapor deposition on a Si3N4 cantilever and shows high frequency responce. **Wire** and **film** type probe shows intermediate characteristics between them. DC and Lock-in measurement method shown in Fig. 4 were used for cases of good and poor signal to noise ratio, respectively. Topological and thermal **image** of biased ITO resistor in Fig. 5 were taken by **wire** and **film** type T.C. cantilever with DC method in air. The size of the ITO is 20.MU.m and spatial resolution of the thermal **image** exceeds that of the infrared thermal microscope. MOSFET in Fig. 6 was scanned by the thin film type T.C. cantilecer in air. Since the MOSFET was shorted near the bottom of gate electrode, heat generation takes place there instead of the region between drain and source. Although concentric temperature distribution is expected in the thermal **image**, measured distribution is distorted to downward. Because the heat conduction through air is dominant in heat transfer between the sample and the probe, and also the shape of the fin film T.C. probe is not symmetric to contact point, the thermal **image** becomes blurred and distorted. In order to eliminate the effect of air the AFM was operated in a vacuum chamber. (author abst.)

34/3,AB/15 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03073754 JICST ACCESSION NUMBER: 96A1016918 FILE SEGMENT: JICST-E

Ferroelectric **Oxide** Thin **Films** and Their Applications to Devices.
OKUYAMA MASANORI (1)
(1) Osaka Univ., Fac. of Eng. Sci.
Hyomen Kagaku(Journal of the Surface Science Society of Japan), 1996, VOL.17,NO.11, PAGE.648-653, FIG.7, REF.15
JOURNAL NUMBER: F0940BAL ISSN NO: 0388-5321
UNIVERSAL DECIMAL CLASSIFICATION: 539.23:54-31 621.383
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Review article
MEDIA TYPE: Printed Publication
ABSTRACT: This paper outlines thin film preparation techniques for ferroelectric substances with D-E hysteresis, large dielectric constant, remarkable piezoelectric effect, pyroelectric effect, and electrooptic effect. Then, this paper introduces functional electron devices using thin films such as DRAM, nonvolatile memory element, low driving voltage thin film EL element, Si monolithic ultrasonic sensor, pyroelectric type infrared ray FET, infrared ray **image** sensor element, optical modulator, optical switch, optical deflection element, micromotor, and optical-drive micro cantilever.

34/3,AB/16 (Item 7 from file: 94)

02795158 JICST ACCESSION NUMBER: 96A0159533 FILE SEGMENT: JICST-E
New Imaging Technologies in Multimedia Era. Gigabit Semiconductor Memories.
SHIMOHIGASHI KATSUHIRO (1)
(1) Hitachi, Ltd.
Gazo Denshi Gakkaishi(Journal of the Institute of Image Electronics Engineers of Japan), 1995, VOL.24,NO.6, PAGE.682-688, FIG.6, REF.9
JOURNAL NUMBER: S0815AAG ISSN NO: 0285-9831
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The age of semiconductor memory of gigabit capacity will surely come at the beginning of the twenty-first century. The history of the integrationof the semiconductor memory is reviewed, focusing on the highest integration such as dyamic, random access memory (DRAM), and development trends of advanced technology and applied technology toward the coming gigabit age are discussed. The gigabit DRAM develops to the memory medium for multi-media and various digital information can be recorded accompanied with higher integration to character, voice, picture and **image**. The development of the portable equipment accelerates the needs of nonvolatile RAM, and non-volatilization of DRAM using ferroelectric material becomes a focal point in the gigabit age. In addition, this paper also describes future of process, device technology and future of the circuit technique.

34/3,AB/17 (Item 8 from file: 94)

02563226 JICST ACCESSION NUMBER: 95A0540777 FILE SEGMENT: JICST-E
Optical semiconductor inspection method.
NISHIOKA KATSUYA (1)

12/20/2002

(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1995, VOL.13,NO.37, PAGE.5-7, FIG.3
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.08 621.383:535.35
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Quality identification of LED lamps is executed by the appearance inspection of lead **wires** and resin **coated** part them using visual or **image** processing application methods. However, stabilized quantitative inspection is hard to execute. This technology is a improved pattern matching method, in which quality identification is executed by comparing the detected value with the good qualityu identification standard value. Automatic inspection will be possible without passing by defects.

34/3,AB/18 (Item 9 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02558969 JICST ACCESSION NUMBER: 95A0831006 FILE SEGMENT: JICST-E
Characterization of Metal/Ferroelectric/Insulator/Semiconductor Structure with CeO2 Buffer Layer.
TERAMOTO K (1); NAGASHIMA K (1); KOIKE H (1); TARUI Y (1); HIRAI T (2)
(1) Waseda Univ., Tokyo, JPN; (2) Asahi Chemical Ind. Co., Ltd., Shizuoka, JPN
Jpn J Appl Phys Part 1, 1995, VOL.34,NO.8A, PAGE.4163-4166, FIG.6, TBL.2, REF.9
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382:537.311.4+ 621.382.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A PbTiO3 ferroelectric film 813 .ANGS. thick was grown on a CeO2/Si(100) substrate by the digital chemical vapor deposition method. As the buffer layer between the perovskite PbTiO3 film and Si substrate, a CeO2 intermediate layer was grown on the Si(100) substrate using an ultrahigh vacuum (UHV) system. The density of surface states at the CeO2/Si(100) interface was estimated from the capacitance-vs-voltage (C-V) characteristics of Al/CeO2/ Si(100) samples to be 8 x 1011/cm2 eV, and CeO2 films on Si(100) are therefore expected to be suitable as gate oxides for metal/ferroelectric/semiconductor-field-effect transistors (FETs). Experimental results derived from the C-V characteristics of metal/ferroelectric/insulator/semiconductor (MFIS)-structured samples show that the MFIS structure has ferroelectric switching properties, as demonstrated by the roughly 2.4 V threshold hysteresis in its C- V characteristics ("memory window"). Furthermore the retention time of the MFIS sample was estimated to be 100,000 s by measuring the time dependence of capacitance at the voltage at the centuer of the memory window. Interfacial lines of the MFIS structure were clear in a transmission electron microscope **image**, and an armorphous CeOx layer and an amorphous SiO2 layer were seen between the Si substrate and PbTiO3 film. Secondary ion mass spectroscopy revealed that there was little diffusion of Si atoms into the PbTiO3 layer on the CeO2 /Si substrate. (author abst.)

34/3,AB/19 (Item 10 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02231364 JICST ACCESSION NUMBER: 94A0769721 FILE SEGMENT: JICST-E
Special Issue for Electronics. Development and Applications of CMOS Process.
YAMANAKA KEIZO (1); MATSUMOTO TOSHIYUKI (1); OKUMURA NOBUO (1); HIROTA YOSHIHIRO (1)
(1) Sumitomo Met. Ind., Ltd., Kenkyu Kaihatsu Honbu
Sumitomo Kinzoku(Sumitomo Metals), 1994, VOL.46,NO.3, PAGE.82-88, FIG.13, TBL.3, REF.6
JOURNAL NUMBER: F0317AAM ISSN NO: 0371-411X CODEN: SUKIA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: LSI technology is considered to be one of the foundation industries supporting the electronics industry. It is a technology that integrate all fields including materials, manufacturing equipment, processes, devices and circuit design. Research into semiconductor processing is essential in the light of supporting semiconductor manufacturing equipment and semiconductor materials which also make up the core of our company's and the groups electronics businesses. We described the state of development of the CMOS process, the basis of LSI technology and examples of its use in electronics applications. The CMOS process involves the construction a 0.8.MU.m twin well, a 1-layer polycide and a 2-**layer** metal **wiring**. We describe LSI's for evaluating defects in Si wafers, the basic material of LSI; technologies for evaluating plasma damage during the process of the semiconductor manufacturing equipment and an example of the use of a prototype KSI for **image** processing presently being used in ASIC operations.

34/3,AB/20 (Item 11 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01988061 JICST ACCESSION NUMBER: 94A0261241 FILE SEGMENT: JICST-E
Image Processing of Superhigh Speed Phenomena.
EZUMI HIROMICHI (1); KEITOKU SUSUMU (2)
(1) Hiroshima-Denki Inst. of Technology, Faculty of Engineering; (2) Hiroshima Women's Univ., Faculty of Home Economics
Hiroshima Denki Daigaku, Hiroshima Jidosha Kogyo Tanki Daigaku Kenkyu Hokoku(Memoirs of the Hiroshima-Denki Institute of Technology and the Hiroshima Junior College of Automotive Engineering), 1993, VOL.26, PAGE.1-6, FIG.11, TBL.1, REF.10
JOURNAL NUMBER: Z0846AAR ISSN NO: 0286-0562
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3 539.23.07
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The plume dynamics of YAG-laser-ablated material from a PbTiO3 target into background gas pressures has been studied by the use of a superhigh speed **image** converter camera, with a framing speed of 2*107 frames/s and a streak speed of 1ns/mm. The photographs obtained by the superhigh speed **image** converter camera were analysed by the **image** processing procedure. The results show that: (i) the

plume initially propagates one-dimensionally with the velocity of(6-8)*105m/s for a distance 2.4mm from target, followed by a 3-dimensional expansion; (ii) in background gas of more than 0.5 Torr, the ablated particles with the velocity of 1.8*106m/s in the plume form a shock wave due to gas collisions. (author abst.)

34/3,AB/21 (Item 12 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01493596 JICST ACCESSION NUMBER: 92A0084974 FILE SEGMENT: JICST-E
Packaging technology in compact type video movie NV-S9.
NISHITANI NOBUYUKI (1); FUJISAKU MINORU (1)
(1) Matsushita Electric Industrial Co., Ltd.
Erekutoronikusu Jisso Gijutsu(Electronic Packaging Technology), 1992, VOL.8,NO.1, PAGE.47-53, FIG.10, TBL.6
JOURNAL NUMBER: L0322AAG ISSN NO: 0911-3053
UNIVERSAL DECIMAL CLASSIFICATION: 621.397.61
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper introduces the products of two printed wiring boards (80*80cm2) on which the packaging density of 10 points/cm 2 at (about 130cm2) was applied. High-density packaging design criterion was constructed in a high-density thin plate four-**layered** printed **wiring** board.18 pieces of 1005 chip R, 420 pieces of the same size C, and 0.5mm pitch QFPIC were mounted on the SMT miniaturized part. This paper also reports the applied double face reflow method and the packaging device.

34/3,AB/22 (Item 13 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01320397 JICST ACCESSION NUMBER: 91A0737782 FILE SEGMENT: JICST-E
An Optoelectronic Device Using Au-Diffused Pb2CrO5 Thin-Films.
TODA KOJI (1); YOSHIDA SHINZO (1)
(1) National Defense Academy
Denshi Joho Tsushin Gakkai Ronbunshi. C,2(Transactions of the Institute of Electronics, Information and Communication Engineers. C-2), 1991, VOL.74,NO.8, PAGE.627-634, FIG.13, TBL.1, REF.11
JOURNAL NUMBER: L0196AAD ISSN NO: 0915-1907
UNIVERSAL DECIMAL CLASSIFICATION: 621.383.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
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34/3,AB/23 (Item 14 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01103404 JICST ACCESSION NUMBER: 90A0848503 FILE SEGMENT: JICST-E
Development and test trial of camera-casette recorder.
HIKISHIMA NAOKI (1); TSUTSUMI MAKOTO (1); HATORI MASASHI (1); SAITO AKIHIKO (1); KITANO YUTAKA (2); SHIMIZU TOSHIO (2); HORI SADATOSHI (2); OTSUKA MASAHIKO (2); TAKEO SEIJI (2)

(1) NEC Home Electronics Ltd.; (2) NEC Corp.
NEC Giho(NEC Technical Journal), 1990, VOL.43,NO.9, PAGE.97-112, FIG.25, TBL.4
JOURNAL NUMBER: G0475BAB ISSN NO: 0285-4139
UNIVERSAL DECIMAL CLASSIFICATION: 621.397.61
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: NEC has developed a new model camcoder. This camcoder is composed of a camera with eightfold zoom lens, and of a VCR of SVHS-C. The camera uses the TTL method. This method enables the camera to control automatically the focusing mechanism of the lens by integration of high frequency signal factor, and to optimize white-balance of **image** signal by sensing color-difference. The VCR has a digital memory device which enables the camera to reduce noise from the **image** signal, and to provide an electronic mechanism for fourfold zoom **image**. The camcoder employs the 1608-size chip element and QFP(Quadruple Flat Package) LSI. These are installed on a two or four **layered** FWB (Printed **Wiring** Board) with 2.54mm spacing distance between signal lines. Consequently, this method, devices and packaging make the camcoder simple and compact in appearance, and also, light in weight. (author abst.)

34/3,AB/24 (Item 15 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01075600 JICST ACCESSION NUMBER: 90A0497824 FILE SEGMENT: JICST-E
Case study. Mounting technology for CCD-TR55.
MINOMIYA TAKEO (1); TOYOFUKU KENJI (1)
(1) Sony Corp.
Sakitto Tekunoroji(Electronic Circuit & Packaging Technology), 1990, VOL.5,NO.3, PAGE.147-150, FIG.5, REF.5
JOURNAL NUMBER: X0497AAN ISSN NO: 0914-8299
UNIVERSAL DECIMAL CLASSIFICATION: 621.397.61
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: On the technology which enabled 8mm CCD color television camera "CCD-TR55" to be smaller and lighter, this paper describes fine pattern printed board consisted of thin four **layers**, **wiring** components, miniatuarization technique of device and SMT problem. An average of 10cm2 packaging density became possible by the adoption of a thin board 4 layer glass epoxy circuit board, and the wired area occupied in circuit boards was reduced to 1/2 of that of conventional one.

34/3,AB/25 (Item 16 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00117728 JICST ACCESSION NUMBER: 85A0365821 FILE SEGMENT: JICST-E
EL display with perovskite type **oxide** thin **films**.
KUWATA JUN (1); FUJITA YOSUKE (1); MATSUOKA TOMIZO (1); NISHIKAWA MASAHIRO (1); TOHDA TAKAO (1); ABE ATSUSHI (1)
(1) Matsushita Electric Industrial Co., Ltd.
Denshi Tsushin Gakkai Gijutsu Kenkyu Hokoku, 1985, VOL.85,NO.32,

PAGE.1-7(ED85-6), FIG.8, TBL.1, REF.10
JOURNAL NUMBER: S0532BAP
UNIVERSAL DECIMAL CLASSIFICATION: 621.385:621.397 621.383:535.35
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

34/3,AB/26 (Item 17 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00081526 JICST ACCESSION NUMBER: 85A0247025 FILE SEGMENT: JICST-E
Surface problem in imaging devces.
HATANAKA YOSHINORI (1)
(1) Shizuoka Univ., Res. Inst. of Electronics
Hyomen Kagaku(Journal of the Surface Science Society of Japan), 1985, VOL.6,NO.1, PAGE.29-36, FIG.16, REF.19
JOURNAL NUMBER: F0940BAL ISSN NO: 0388-5321
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS 621.385.83
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

34/3,AB/27 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

03138328 EDB-91-075763
Title: Bubbly flow velocity measurements near a heated cylindrical conductor
Author(s): Canaan, R.E.; Hassan, Y.A. (Texas A M Univ., College Station (USA))
Conference Title: American Nuclear Society (ANS) winter meeting
Conference Location: Washington, DC (USA) Conference Date: 11-15 Nov 1990
Source: Transactions of the American Nuclear Society (USA) v 62. Coden: TANSA ISSN: 0003-018X
Publication Date: 1990
p 632-634
Report Number(s): CONF-901101--
Language: In English
Abstract: The objective of this study is to apply recent advances and improvements in the digital pulsed laser velocimetry (DPLV) technique to the analysis of two-phase bubbly flow about a cylindrical conductor emitting a constant heat flux within a transparent rectangular enclosure. Pulsed laser velocimetry is a rapidly advancing fluid flow visualization technique that determines full-field instantaneous velocity vectors of a quantitative nature such that the flow field remains undisturbed by the measurement. The DPLV method offers several significant advantages over more traditional fluid velocity measurement techniques such as hot **wire/film** anemometry and laser Doppler anemometry because reliable instantaneous velocity data may be acquired over substantial flow areas in a single experiment.

34/3,AB/28 (Item 2 from file: 103)
DIALOG(R)File 103:Energy SciTec

12/20/2002

02068177 NOV-88-086355; EDB-88-010897
Author(s): Dorman, A.; Glave, W.K.; Birnbach, C.
Title: **Solid-state** X-ray receptor and method of making same
Patent No.: US 4700076
Patent Assignee(s): Digital Imaging Co. of America, Inc., Hauppauge, NY
Patent Date Filed: Filed date 2 Sep 1983
Publication Date: 13 Oct 1987
p v
Language: English
Abstract: A receptor for X-radiation to produce electrical signals representative of an X-ray **image** is described comprising: at least one support comprised of a ceramic board having surfaces for supporting electrical conducting leads and circuit means; and a linear array of semiconductor elements supported on the ceramic board and positioned to receive impinging X-radiation and to produce electrical signals in response thereto. There are plural electrical conducting leads supported on at least one surface of the ceramic board; means for coupling the electrical signals produced by respective ones of the semiconductor elements to at least one of the electrical conducting leads; output terminal means supported on the ceramic board to provide output **image** signals; and circuit means supported on the ceramic board for coupling the electrical signals from the at least one electrical conducting **lead** to the output terminal means. The electrical conducting leads supported on the surface of the ceramic board project beyond the edge of the ceramic board and the array of semiconductor elements is supported between the edge of the ceramic board and the projections of the electrical conducting leads.